A Tribute to Jim Williams

Linear Technology Magazine (1991-2011)

The LT1074 Family of Step Down Switching Regulators

by Jim Williams

A substantial percentage of DC regulator requirements involve reduction or step down of a primary voltage. Linear regulators do this, but they don't achieve the efficiency of switchers. The theory supporting step down or "buck" switching regulation is well established, and has been exploited for some time. However, conveniently applied ICs allowing practical implementations haven't been available. A new power IC device, the LT1074, permits broad application of step down regulators with minimal complexity and low cost. Further, more complex step down regulator functions are possible with it also.

The LT1074 is a 5A bipolar switching regulator requiring minimal external parts for operation. While the block diagram of Figure 1. reveals a complex device, basic operation is still fairly straightforward. A description of the main circuit elements and their pin functions is as follows.

The LT1074 uses a special controlled saturation Darlington NPN output switch, with the emitter out-

continued on page 8

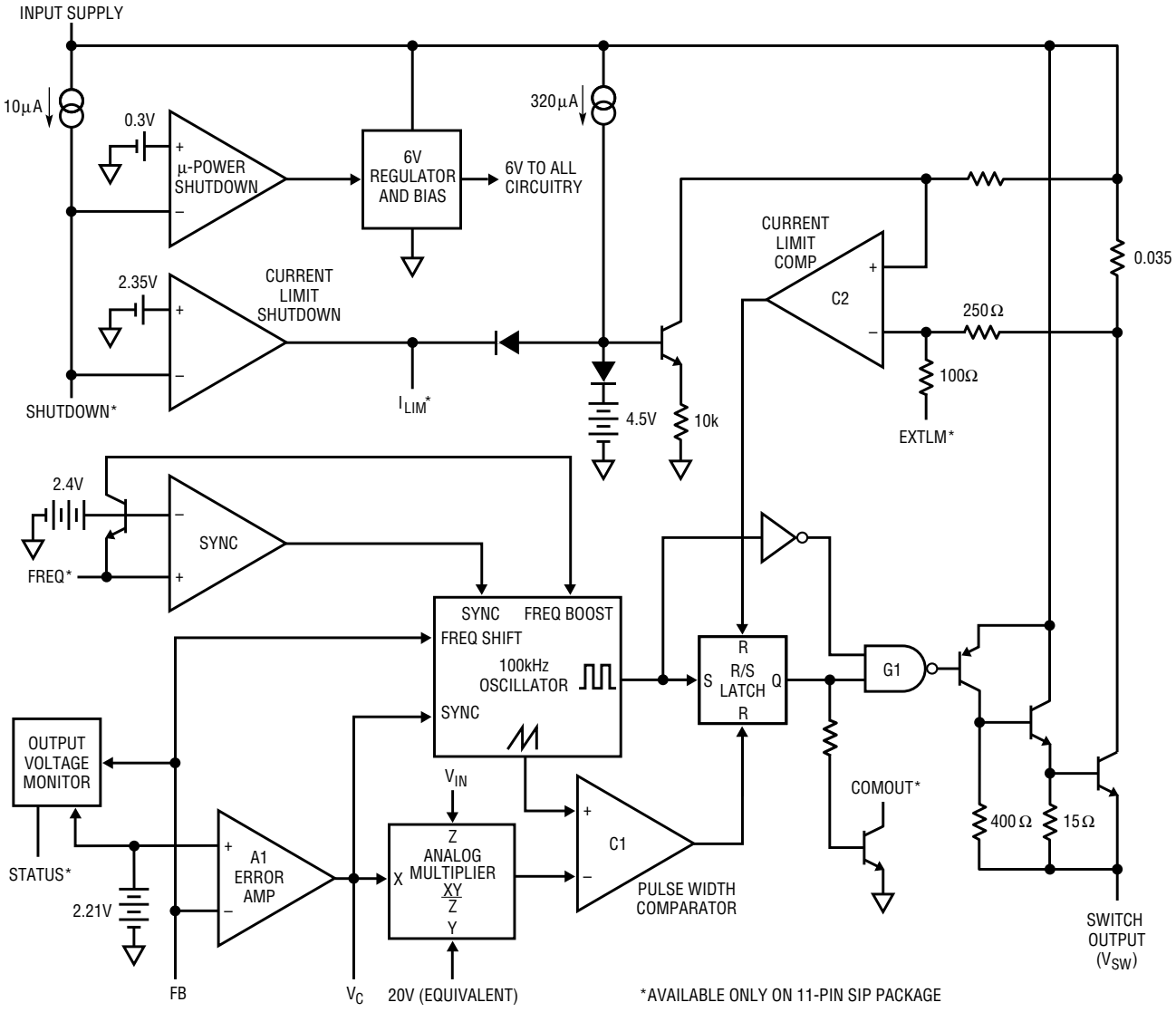


Figure 1. LT1074/LT1076 Block Diagram

continued from page 7

put at pin VSW. This switch uses an isolated design, allowing voltage swings up to 40V below the ground pin. In addition, the switch also has a continuous current monitor. The oscillator of the LT1074 operates at 100kHz, driving the switch through a control latch. Duty cycle control comes from a pulse width comparator, which in turn is driven by the main error amplifier through the analog multiplier. This multiplier allows a loop gain independent of input voltage, optimizing transient response. The error amp of the LT1074 compares a sample of the output presented to the FB pin to an internal 2.21V (±2.5%) reference. Loop compensation is accomplished by a simple RC network at the amplifier output (VC pin), to ground.

While the above describes the basic operational loop of the LT1074 design, accessory internal functions also exist. These are I_{LIM}, FREQ, STATUS, COMOUT, SHUTDOWN and EXTLIM pins (available only in the 11 pin package). As alluded, there are multiple power packages used with the LT1074., a 4 lead TO-3 (K), a 5 lead TO-220 (T), and the 11 lead SIP package (V), which permits the optional clock synchronization, micropower shutdown, current limit programming and other features. The LT1074 is available in two basic voltage grades, the LT1074 for 45V(max) inputs, and the LT1074HV, usable to 64V. There is also a 2.5A rated device, the LT1076.

Applications

Figure 2 is a practical LT1074 voltage step down or "buck" circuit, using minimum componentry. It closely follows a voltage step down conceptual model, described as follows.

When the LT1074 (internal) switch closes, input voltage appears at the inductor, and current flowing through the inductor-capacitor combination builds over time. When the switch opens, current flow ceases and the magnetic field around the inductor collapses. Faraday teaches that the voltage induced by the collapsing magnetic field is opposite to the originally applied voltage. As such, the voltage at the inductor's left end heads negative, and is clamped by the diode. The charge accumulated on the capacitor has no discharge path, leaving an output DC potential. This potential is lower than the input, because the inductor limits current during the switch on-time.

Ideally, there are no dissipative elements in this voltage step down conversion. Although the output voltage is lower than the input, there is no energy lost in this conversion. In practice, the circuit elements do have losses, but step down efficiency is still higher than with inherently dissipative (e.g. voltage divider) approaches. In this circuit, feedback controls the switch, to regulate output voltage. The switch on-time (e.g. inductor charge time) is varied to maintain the output against changes in either input or loading.

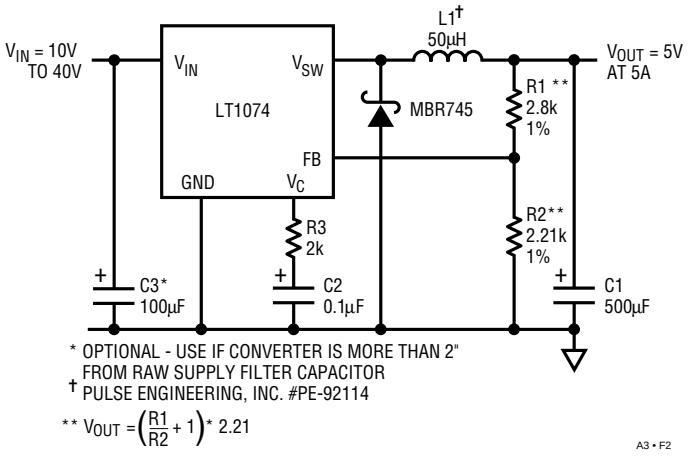


Figure 2. LT1074 Step Down Regulator (5V output)

With respect to a practical circuit using the LT1074 regulator, some additional new elements appear. The RC components at the LT1074 VC pin provide frequency compensation, stabilizing the feedback loop. Output sensing resistors R1/R2 are selected to scale the output to the desired voltage V_{OUT}, generally as noted in the figure, with values shown in this case for 5V.

Performance wise, the circuit operates over an input range of 10-40V, and has a maximum output of 5A. Efficiency is about 80% at a current of 1A, while output ripple is about 25mV with the filtering as shown. With these and other switching regulators, power components are critical to performance, and should be rated for switching use at the currents anticipated.

Regulated negative outputs with the LT1074 are easily obtained also, using a simple two terminal inductor. The basic positive to negative converter of Figure 3 demonstrates this, essentially grounding the inductor, steering diode current to what is now a negative output. This design accomplishes the plus-to-minus DC level shift by connecting the LT1074 GND pin direct to the negative output, requiring an isolated heat sink.

Feedback is sensed from the grounded positive output terminal, and the regulator again forces its feedback pin 2.21V above its GND pin. Output voltage scaling is numerically as in Figure 2, with a negative sign. Circuit ground is common to input and output, making system use easy.

Overall performance is as noted, and is similar to the positive buck converter of Figure 2, but with some unique distinctions. On the plus side, note that the input/output voltages of this configuration are seen in se-

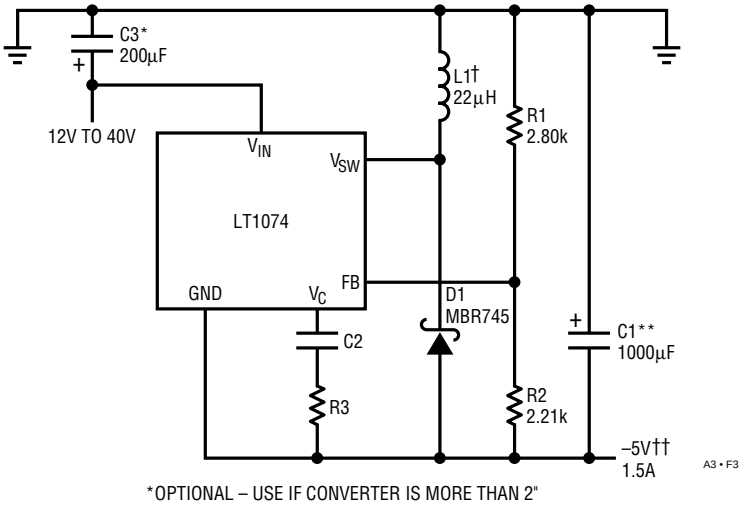
continued on page 9

continued from page 8

ries by the LT1074, as V_{IN}. This has the effect of allowing a very low absolute level for the positive input, down to as low as 5V, making the circuit an efficient 5V to -5V power converter. On the down side, note in this instance the LT1074 control pins are floating off ground, presenting some potential problems with control interfacing (when necessary).

Figure 4, another variant, is used when it is desirable to operate the case (GND) pin of the regulator at common. This option uses an op amp as a precision feedback level shifter. A1 facilitates loop closure, providing a scaled inversion of the negative output to the LT1074 FB pin. Precision resistors R1/R2 set negative output voltage as noted (values shown for a -5V output). The VC pin of the LT1074 is left open, and the RC network around A1 gives frequency compensation.

Advantages of this circuit compared to Fig. 3 is that the LT1074 package can directly contact a grounded heat sink. Additionally, this circuit permits ground referred addressing of the regulator's control pins. Disadvantages are that it requires a higher minimum input voltage, plus an additional active device..



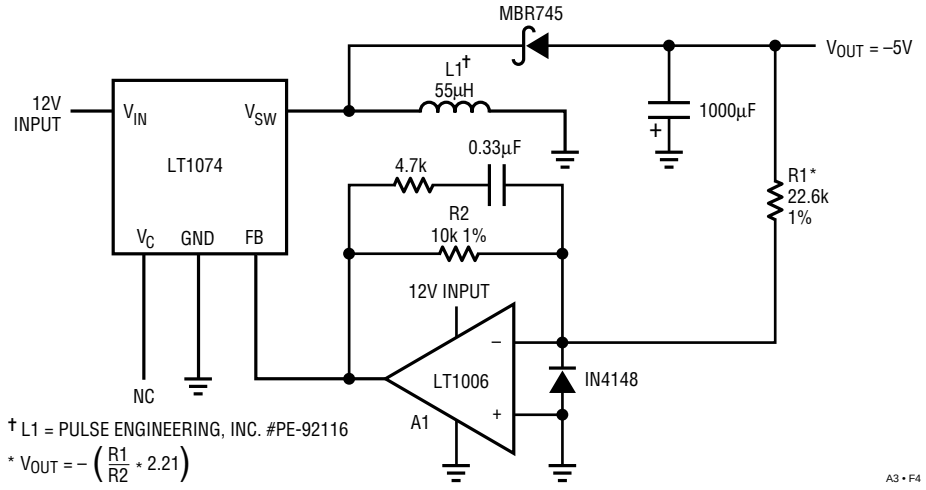
*OPTIONAL – USE IF CONVERTER IS MORE THAN 2" FROM RAW SUPPLY FILTER CAPACITOR

**LOWER OUTPUT RIPPLE CAN BE OBTAINED BY PARALLELING SEVERAL LOWER VALUE CAPACITORS. AN OUTPUT FILTER OF 5µH, 100µF WILL GIVE 20:1 RIPPLE ATTENUATION WITH AN ESR OF 0.1Ω ON THE 100µF CAPACITOR

†PULSE ENGINEERING, INC. #PE-51590

††MAXIMUM OUTPUT CURRENT IS 1.5A AT V_{IN} = 5V 3A AT V_{IN} = 15V AND 3.5A AT V_{IN} = 30V

Figure 3. Positive to Negative Converter



† L1 = PULSE ENGINEERING, INC. #PE-92116

* $V_{OUT} = -\left(\frac{R1}{R2} * 2.21\right)$

Figure 4. Positive to Negative Converter with Op Amp Level Shift

Higher Output Currents with Tapped Inductors

Buck (step-down) convertors have a switch current at least as high as regulator output current. This limits LT1074 output current to 5A in the simple buck convertor topology. A slightly modified version (shown on the data sheet) can double available output current to 10A when input voltage is a minimum of 20V. The modified version uses a 3 to 1 tapped inductor which generates current gain in the inductor.

During switch "on" time current flows through the entire inductor to the output and can have a maximum value of 5A. When the switch turns off, the voltage at the tap flies negative and current flows to the output through just 1/4 of the inductor. Energy conservation requires that this current be four times the current which was flowing in the entire inductor. Average current delivered to the output is between 5A and 20A, as determined by operating switch duty cycle. For low input voltages, switch duty cycle is very high, and maximum output current is only slightly above 5A. For input voltage above 20V, duty cycle is low enough to deliver 10A output current.

The voltage on the LT1074 switch pin flies negative to about 17V during switch "off" time due to the transformer action of the inductor. Leakage inductance, however, would cause, at switch turn-off, the switch voltage to briefly fly negative without limit. Clamps are needed to protect the LT1074.

An LT1123 Ultra Low Dropout 5V Regulator

Jim Williams and Dennis O'Neill

Switching regulator post regulation, battery powered apparatus, and other applications often require low V_{IN}-V_{OUT}, or dropout, linear regulators. For post regulators this is needed for high efficiency. In battery circuits lifetime is significantly effected by regulator dropout. The LT1123, a new low cost reference/control IC, is designed specifically for cost-effective duty in such applications. Used in conjunction with a discrete PNP power transistor, the 3 lead TO-92 unit allows very high performance positive leg regulator designs. The IC contains a 5V bandgap reference, error amplifier, NPN darlington driver, and circuitry for current and thermal limiting.

A low dropout example is the simple 5V circuit of Fig. 1, using the LT1123 and an MJE1123 silicon PNP. In operation, the LT1123 sinks Q1 base current through the DRIVE pin, to servo control the FB (feedback) pin to 5V. R1 provides pull-up current to turn Q1 off, and R2 is a drive limiter. The 10µF output capacitor (Cout) provides frequency compensation. The LT1123 is designed to tolerate a wide range of capacitor ESR so that low cost aluminum electrolytics can be be used for C_{OUT}. If the circuit is located more than 6 inches from the input source, the optional 10µF input capacitor (C_{IN}) should be added.

Normally, such configurations require external protection circuitry. Here, the MJE1123 has been cooperatively designed by Motorola and LTC for use with the LT1123. The device is specified for saturation voltage for currents up to 4 amperes, with base drive equal to the minimum LT1123 drive current specification. In addition, the MJE1123 is specified for min/max beta at high current. Because of this factor and the defined LT1123 drive, simple current limiting is practical. In limit, excessive output current causes the LT1123 to drive Q1 hard until the LT1123 current limits. Maximum circuit output current is then a product the LT1123 current and the beta of Q1. The foldback characteristic of the LT1123's drive current combined with the MJE1123 beta and safe area characteristics provide reliable short circuit limiting. Thermal limiting can also be accomplished, by mounting the active devices with good thermal coupling.

Performance of the circuit is notable, as it has lower dropout than any monolithic regulator. Line and load regulation are typically within 5 millivolts, and initial accuracy is typically inside 1%. Additionally, the regulator is fully short circuit protected, with a no load quiescent current of 1.3mA.

Figure 2 shows typical circuit dropout characteristics, in comparison with other IC regulators. Even at 5A the LT1123/MJE1123 circuit dropout is less than 0.5V, decreasing to only 50mV at 1A. Totally monolithic regulators cannot approach these figures, primarily because their power transistors do not offer the MJE1123 combination of high beta and excellent saturation. For example, dropout is ten times lower than in 138 types, and significantly better than all the other IC types. Because of Q1's high beta, base drive loss is only 1-2% of output current even at high output currents. This maintains high efficiency under the low V_{IN}-V_{OUT} conditions the circuit will typically see. As an exercise, the MJE1123 was replaced with a 2N4276 germanium device. This provided even lower dropout performance, but limiting couldn't be production guaranteed without screening.

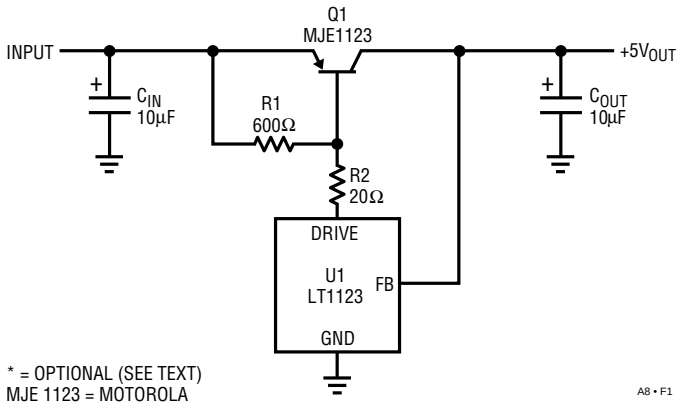


Figure 1. The LT1123 5V regulator features ultra-low dropout.

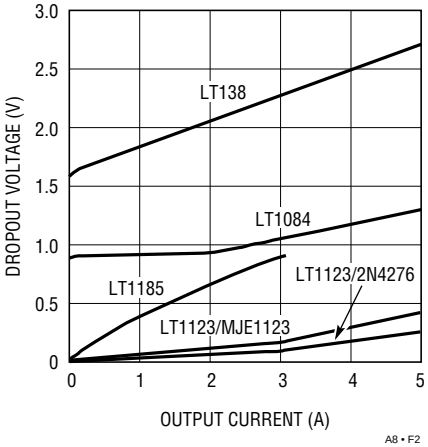


Figure 2. LT1123 regulator dropout voltage vs. output current

Ultra-low Noise and Low Drift Chopped-FET Amplifier

by Jim Williams

Figure 1's circuit combines the extremely low drift of a chopper-stabilized amplifier with a pair of low noise FETs. The result is an amplifier with 0.05µV/°C drift, offset within 5µV, 100pA bias current and 50nV noise in a 0.1Hz–10Hz bandwidth. The noise performance is especially noteworthy; it is almost 35 times better than monolithic chopper-stabilized amplifiers.

FETs Q1 and Q2 differentially feed A2 to form a simple low-noise op amp. Feedback, provided by R1 and R2, sets closed-loop gain (in this case 10,000) in the usual fashion. Although Q1 and Q2 have extraordinarily low noise characteristics, their offset and drift are uncontrolled. A1, a chopper-stabilized amplifier, corrects these deficiencies. It does this by measuring the difference between the amplifier's inputs and adjusting Q1's channel current via Q3 to minimize the difference. Q1's skewed drain values ensure that A1 will be able to capture the offset. A1 and Q3 supply whatever current is required to force offset to within 5µV into Q1's channel. Additionally, A1's low bias current does not appreciably add to the overall 100pA amplifier bias current. As shown, the amplifier is set up for a non-inverting gain of 10,000, although other gains and inverting operation are possible. Figure 2 is a plot of the measured noise performance.

The FETs' Vgs can vary over a 4:1 range. Because of this, they must be selected for 10% Vgs matching. This matching allows A1 to capture the offset without introducing any significant noise.

Figure 3 shows the response (trace B) to a 1mV input step (trace A). The output is clean, with no overshoots or uncontrolled components. If A2 is replaced with a faster device (e.g. LT1055) speed increases by an order of magnitude with similar damping. A2's optional overcompensation can be used (capacitor to ground) to optimize response for low closed loop gains.

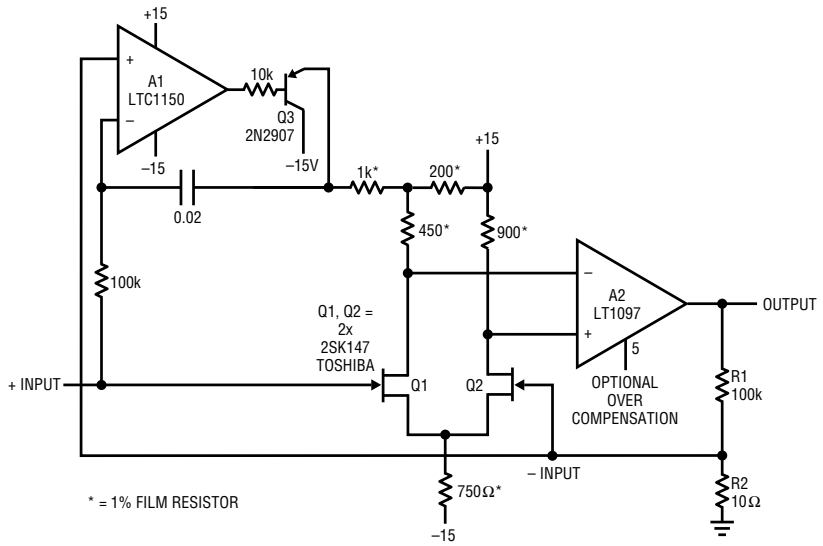


Figure 1. Chopper Stabilized FET Pair Combines Low Bias, Offset and Drift with 45nV Noise

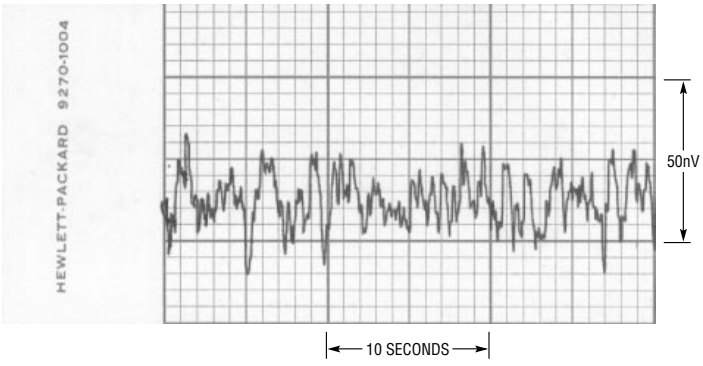


Figure 2. 45nV Noise Performance for Figure 1. A1's Low Offset and Drift are Retained, but Noise is Almost 35 Times Better

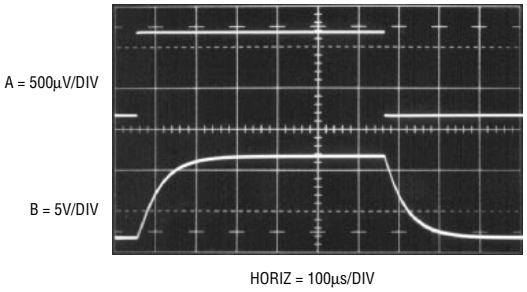


Figure 3. Step Response for the Low Noise +10,000 Amplifier. A 10x Speed Increase is Obtainable by Replacing A2 with a Faster Device

LT1109 Generates V_{pp} for Flash Memory

by Steve Pietkiewicz

Flash memory chips such as the Intel 28F020 2Megabit device require a V_{pp} program supply of 12 volts at 30mA. A DC–DC converter may be used to generate 12 volts from the 5 volt logic supply. The converter must be physically small, available in surface-mount packaging, and have logic-controlled shutdown. Additionally, the converter must have carefully controlled rise time and zero overshoot. V_{pp} excursions beyond 14 volts for 20ns or longer will destroy the ETOX[1]-process based device.

Figure 1's circuit is well suited for providing V_{pp} power for a single flash memory chip. All associated components, including the inductor, are surface mount devices. The $\overline{\text{SHUTDOWN}}$ input turns off the converter, reducing quiescent current to 300µA when pulled to a logic 0. V_{pp} rises in a controlled fashion, reaching 12 volts ±5% in under 4ms. Output voltage goes to V_{cc} minus a diode drop when the converter is in shutdown mode. This is an acceptable condition for Intel flash memories and does not harm the memory.

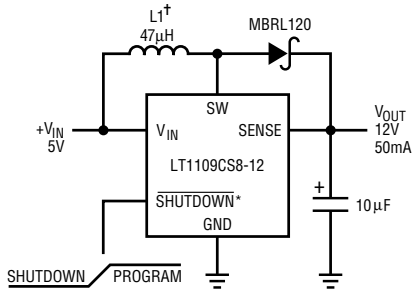


Figure 1. All Surface Mount Flash Memory Vpp Generator

[1]ETOX is a trademark of Intel Corporation.

RF Leveling Loop

by Jim Williams

Leveling loops are often a requirement for RF transmission systems. More often than not, low cost is more important than absolute accuracy. Figure 1 shows such a circuit.

The RF input is applied to A1, an LT1228 operational transconductance amplifier. A1's output feeds A2, the LT1228's current-feedback amplifier. A2's output, the output of the circuit, is sampled by the A3-based gain control configuration. This arrangement closes a gain-control loop back at A1. The 4pF capacitor compensates rectifier diode capacitance, enhancing output flatness vs frequency. A1's I_{SET} input current controls its gain, allowing overall output level control. This approach to RF leveling is simple and inexpensive, and provides low output drift and distortion.

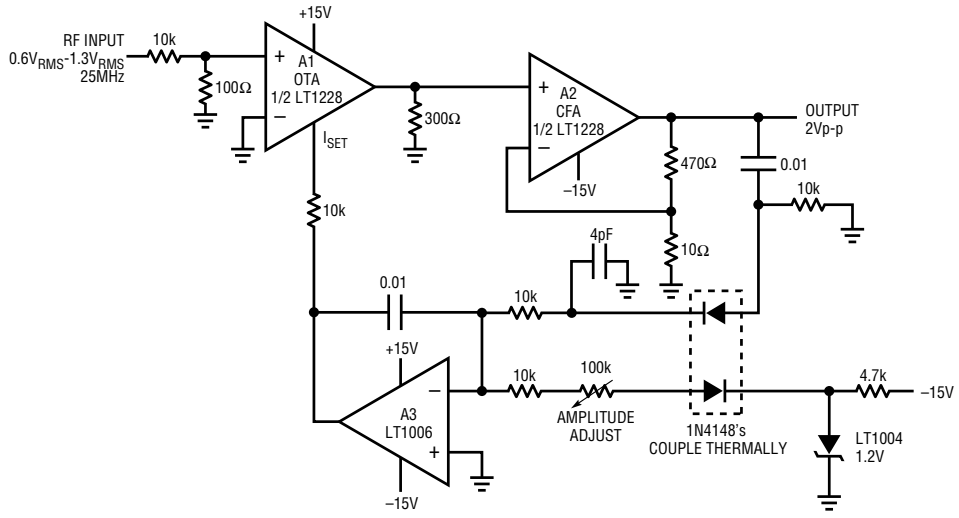


Figure 1. Simple RF Leveling Loop

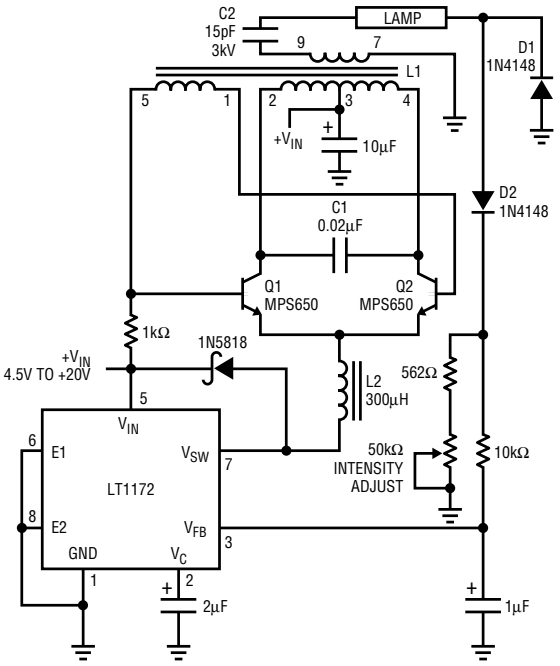
Illumination Circuitry for Liquid Crystal Displays

by Jim Williams

Current-generation portable computers and instruments employ back-lit liquid crystal displays (LCDs). Cold-cathode fluorescent lamps (CCFLs) provide the highest available efficiency for backlighting the display. These lamps operate on high-voltage AC and therefore require efficient high-voltage DC-AC converters. In addition to providing high efficiency, converters used with CCFLs should deliver the lamp drive in the form of a sine wave. This is desirable to minimize RF emissions, which can cause interference with other devices and degrade overall operating efficiency. The circuit should also permit lamp-intensity control from zero to full brightness with no hysteresis or "pop-on."

The LCD also requires a bias supply for contrast control. The supply's negative output should be regulated and should be variable over a considerable range.

Because of their small size and battery-powered operation, LCD-equipped devices require low component count and high efficiency. Size constraints place severe limitations on circuit architecture, and long battery life is usually a priority. Laptop and hand-held portable computers are excellent examples. In these applications, the CCFL and its power supply are responsible for almost 50% of the battery drain. Additionally, these components, including the PC board and all hardware, must usually fit within the LCD enclosure, with a height restriction of 0.25".



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 (GERMAN) RECOMMENDED.
L1 = SUMIDA-6345-020 OR COILTRONICS-CTX110092-1.
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS-CTX300-4
Q1, Q2 = AS SHOWN OR BCP 56 (PHILIPS SO PACKAGE)
DO NOT SUBSTITUTE COMPONENTS

SUMIDA (708) 956-0666
COILTRONICS (305) 781-8900

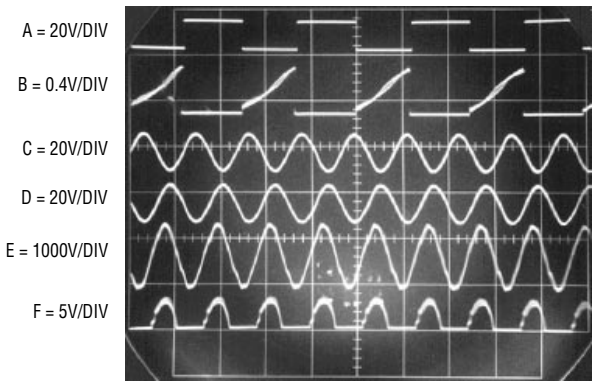
Figure 1. Cold-cathode fluorescent lamp power supply

CCFL Power Supplies

Any discussion of CCFL power supplies must consider lamp characteristics. These lamps are difficult loads to drive, particularly for a switching regulator. They have a "negative resistance" characteristic; the starting voltage is significantly higher than the operating voltage. Typically, the starting voltage is about 600 volts, although higher and lower voltage bulbs are common. Operating voltage is usually 300–400 volts, although other bulbs may require different potentials. Bulb size or length does not necessarily correlate to break-down voltage. The bulbs will operate from DC, but migration effects within the bulb will quickly damage it. Hence, the waveform must be AC with no DC content.

Bulb operating frequencies are typically 20 to 100kHz, and a sine-like waveform is preferred. The sine-like drive has low harmonic content, which minimizes RF emissions that can cause interference and efficiency degradation.

Figure 1's circuit meets CCFL-drive requirements. Efficiency can be as high as 78% with an input voltage range of 4.5V–20V. 82% efficiency is possible if the LT1172 is driven from a low voltage (3–5V) source. Additionally, lamp intensity is continuously and smoothly variable from zero to full



A AND B HORIZ = 10µs/DIV
C THRU F HORIZ = 20µs/DIV
TRIGGERS FULLY INDEPENDENT

Figure 2. CCFL power supply waveforms

intensity. When power is applied, the LT1172 switching regulator's feedback pin is below the device's internal 1.23V reference, resulting in full duty-cycle modulation at the V_{SW} pin (trace A, Figure 2). L2 conducts current (trace B), which flows from L1's center tap, through the transistors, into L2. L2's current is deposited in switched fashion to ground by the regulator's action.

L1 and the transistors comprise a current-driven, Royer-class converter, which oscillates at a frequency determined primarily by L1's characteristics (including its load) and the 0.02µF capacitor. LT1172 driven L2 sets the magnitude of the Q1–Q2 tail current, and hence L1's drive level. The 1N5818 diode maintains L2's current flow when the LT1172 is off. The LT1172's 100kHz clock rate is asynchronous with respect to the push-pull converter's (60kHz) rate, accounting for trace B's waveform thickening.

The 0.02µF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (traces C and D, respectively). L1 furnishes voltage step-up, and about $1400V_{P-P}$ appears at its secondary (trace E). Current flows through the 15pF capacitor into the lamp. On negative waveform cycles, the lamp's current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562Ω–50kΩ potentiometer chain. The positive half-sine appearing across these resistors (trace F) represents 1/2 the lamp current. This signal is filtered by the 10kΩ-1µF pair and presented to the LT1172's feedback pin. This connection closes a control loop which regulates lamp current. The 2µF capacitor at the LT1172's V_C pin provides stable loop compensation. The loop forces the LT1172 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, can be varied with the potentiometer. The constant current drive allows full 0–100% intensity control with no lamp dead zones or "pop-on" at low intensities. Additionally, lamp life is enhanced because current cannot increase as the lamp ages.

Several points should be kept in mind when observing this circuit's operation. L1's high-voltage secondary can only be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast*

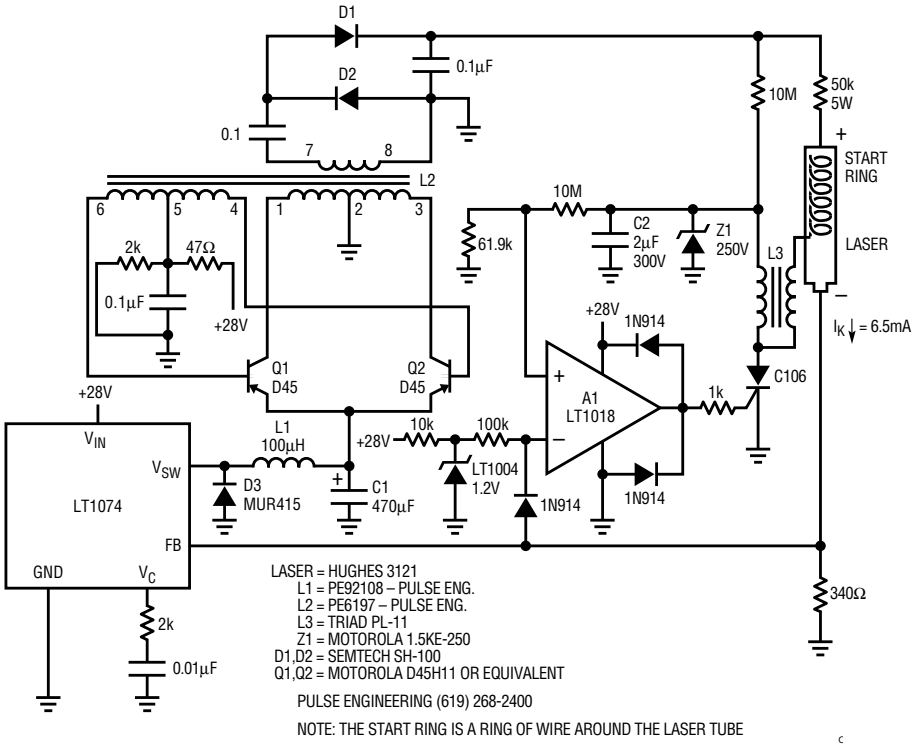


Figure A1. Laser-driver power supply

A Related Circuit: Helium Neon Laser Driver

The high-voltage-compliance current-loop approach of the CCFL power supply is suitable for other applications as well. Current sensing permits precise, high-efficiency control of a wide variety of difficult loads. A HeNe laser is such a load. Lasers are negative impedances operating at very high voltages. Typically, they require from 6 to 10kV to start, with an operating voltage in the 1 to 3kV range. Simple high-voltage drive does not provide this. The circuit in Figure A1 adapts the CCFL circuitry to control a laser. Both tube-current stability and electrical efficiency are improved over the more conventional voltage-mode drive.

Q1 and Q2 combine with L2 to form a self-oscillating DC-DC converter. No resonating capacitor is used in this design. The DC-DC converter operates in square-wave mode, although resonant operation could be used to minimize harmonics. The converter's high-voltage output is multiplied by the D1-D2 voltage doubler and applied to the laser via the 50kΩ ballast resistor. This resistor is required to isolate the laser from the 0.1µF output capacitor. Laser current flow is converted to a voltage by the 340Ω shunt and is fed back to the LT1074 step-down switching regulator. D3, L1, and C1 smooth the LT1074's pulsed output to DC and drive the DC-DC converter. This completes a loop that controls the laser current. The components at the LT1074's V_C pin stabilize the loop. The frequency compensation is arranged so transients (e.g., turn-on) will not cause a brief lowering of the tube current. Such an event will cause laser impedance to rise dramatically, extinguishing the laser.

L2 and the voltage doubler supply a maximum of about 3.5kV, not enough to start laser conduction. A1, L3, and associated components provide a high voltage start-up.

continued on page 7

majority of oscilloscope probes will break down and fail if used for this measurement.[1] Tektronix type P-6009 (acceptable) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

Another consideration involves observing waveforms. The LT1172's switching frequency is completely asynchronous from the Q1–Q2 Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 2 was obtained using a dual-beam oscilloscope (Tektronix 556). LT1172-related traces A and B are triggered on one beam, while the remaining traces are triggered on the other beam. Single-beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used, but are less versatile and are restricted to four traces.

Obtaining and verifying high efficiency requires some diligence.[2] The optimum efficiency values given for C1 and C2 are typical, and will vary for specific types of lamps. C1 sets the circuit's resonance point, which varies to some extent with the lamp's characteristic. C2 ballasts the lamp, effectively buffering its negative-resistance characteristic. Small values of C2 provide the most load isolation, but require relatively large transformer output voltage for loop closure. Large C2 values minimize transformer output voltage, but degrade load buffering. Also, C1's "best" value depends somewhat on the type of lamp used. Both C1 and C2 must be selected for given lamp types. Some interaction occurs, but general guidelines are possible. Typical values for C1 are 0.01 to 0.047µF. C2 usually ends up in the 10pF–47pF range. C1 must be a low-loss capacitor; substitution for the WIMA device is not recommended. A poor-quality dielectric for C1 can easily degrade efficiency by 10%. C1 and C2 are selected by trying different values for each and iterating towards minimum supply input current. During this procedure, ensure that loop closure is maintained by monitoring the LT1172's feedback pin, which should be at 1.23 volts. Several trials usually produce the optimum C1 and C2 values. Note that the highest efficiencies are not necessarily associated with the most aesthetically pleasing waveshapes, particularly at Q1, Q2, and the output.

Other issues influencing efficiency include bulb wire length and energy leakage from the bulb. The high-voltage side of the bulb should have the smallest practical lead length. Excessive length results in radiative losses, which can easily reach 3% for a three-inch wire. Similarly, no metal should contact or be in close proximity to the bulb. This prevents energy leakage, which can exceed 10%. (These considerations should be made with knowledge of other LCD issues. See Appendix B of AN49, "Mechanical Design Considerations for Liquid Crystal Displays.")

Special attention should be given to the layout of the circuit board, since high voltage is generated at the output. The output coupling capacitor must be carefully located to minimize leakage paths on the circuit board. A slot in the board will further minimize leakage. Such leakage can permit current flow outside the feedback loop, wasting power. In the worst case, long term contamination build-up can increase leakage inside the loop, resulting in starved lamp drive or destructive arcing. To minimize leakage, it is good practice to break the silk-screen line which outlines transformer T1. This prevents leakage from the high voltage secondary to the primary. Another technique for minimizing leakage is to evaluate and specify the silk-screen ink for its ability to withstand high voltages.

Once these procedures have been followed, efficiency can be measured. Efficiency may be measured by determining bulb current and voltage. Measuring current involves measuring RMS voltage across the 562Ω resistor (short the potentiometer). The bulb current is

$$I_{BULB} = (E/R) \times 2$$

Multiplication by two is necessary because the diode steering dumps the current to ground on negative cycles. Bulb RMS voltage is measured at the bulb with a properly compensated high-voltage probe. Multiplying these two results gives power in watts, which may be compared to the DC-input-supply E x I product. In practice, the lamp's current and voltage contain

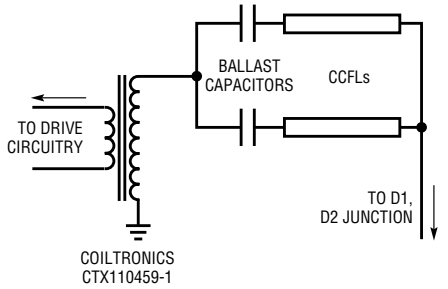
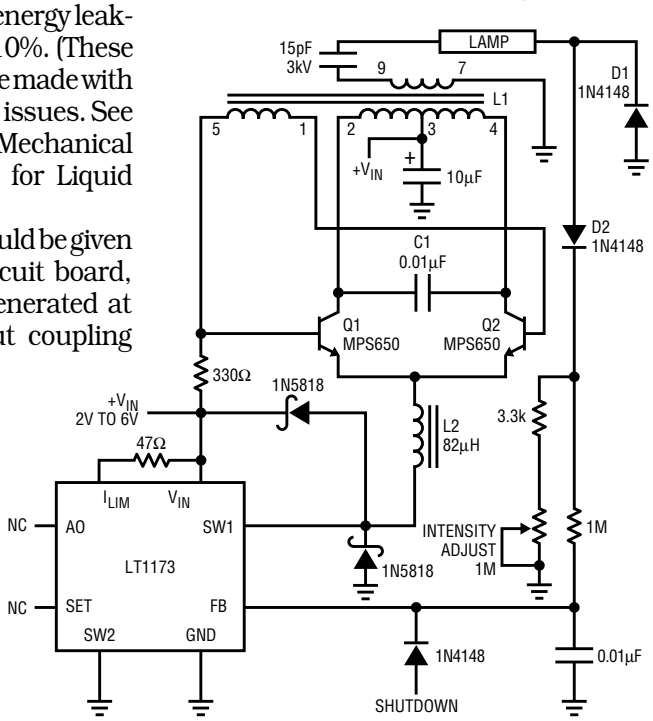


Figure 3. Separate ballast capacitors allow one transformer to drive two tubes



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 (GERMAN) RECOMMENDED.
L1 = SUMIDA-6345-020 OR COILTRONICS-CTX110092-1.
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = TOKO 262LYF-0091K
DO NOT SUBSTITUTE COMPONENTS

Figure 4. Low-current CCFL power supply

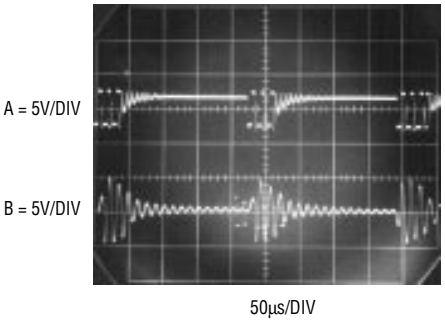


Figure 5. Low-current CCFL power-supply waveforms

small out-of-phase components, but their error contribution is negligible.

Both the current and voltage measurements require a wide-band true-RMS voltmeter. The meter must employ a thermal-type RMS converter—the more common logarithmic-computing type instruments are inappropriate because their bandwidths are too low. (See AN49 for a discussion of the operational theory and limitations of various AC voltmeters.)

The previously recommended high voltage probes are designed to see a 1MΩ, 15–22pF oscilloscope input. The RMS voltmeters have a 10MΩ input. This difference necessitates an impedance matching network between the probe and the voltmeter. Details of this and other efficiency measurement issues appear in Appendix C of AN49, "Achieving Meaningful Efficiency Measurements."

Two-Tube Designs

Some displays require two tubes instead of the more popular single-tube approach. These two-tube designs usually require more power. Accommodating two tubes involves separate ballast capacitors (see Figure 3), but circuit operation is similar. Higher power may require a different transformer rating. Figure 1's transformer can supply 7.5mA, although more current is possible with appropriate transformer types. For reference, an 11mA-capability transformer appears in Figure 3.

Low-Power CCFL Supply

Figure 4 represents the other extreme. This design is optimized for single-tube operation at very low currents. Figure 1's circuit typically drives 5mA maximum, but this design tops out at 1mA. This circuit maintains control down to tube currents of 1µA, a very dim light. It is intended for applications where the longest possible battery life is desired. Maintaining high efficiency at low tube currents requires modifying the basic design.

Achieving high efficiency at low operating currents requires lowering Figure 1's quiescent power drain. To do this, the LT1172, a pulse-width-modulator-based device, is replaced with an LT1173. The LT1173 is a burst-mode-type regulator. When this device's feedback pin is too low, it delivers a burst of output current pulses, putting energy into the transformer and restor-ing the feedback point. The regulator maintains control by appropriately modulating the burst duty cycle. The ground-referred diode at the SW1 pin prevents substrate turn-on due to excessive L2 undershoot. During the off periods, the regulator is essentially shut down. This type of operation limits available output power, but cuts quiescent current losses. In contrast, Figure 1's LT1172 pulse-width-modulator-type regulator maintains "housekeeping" current between cycles. This results in more available output power but higher quiescent currents. Figure 5 shows operating waveforms for the circuit in Figure 4. When the regulator comes on (trace A) it delivers bursts of output current to the L1–Q1–Q2 high-voltage converter. The converter responds with bursts of ringing at its resonant frequency. The circuit's loop operation is similar to that of Figure 1.[3]

LCD Bias Supplies

LCDs also require a bias supply for contrast control. The supply's variable negative output permits adjustment of display contrast. Relatively little power is involved, easing RF radiation and efficiency requirements. The logic sections of display drivers operate from single 5V supplies, but the actual driver outputs swing between +5V and a negative bias potential. Varying this bias varies the contrast of the display.

An LCD bias generator, developed by Steve Pietkiewicz of LTC, is shown in Figure 6. In this circuit U1 is an LT1173 micropower DC-DC converter. The 3V input is converted to +24V by U1's switch, L1, D1, and C1. The switch pin (SW1) then drives a charge pump composed of C2, C3, D2, and D3 to generate –24V. Line regulation is less than 0.2% from 3.3V to 2.0V inputs. Although load regulation suffers somewhat because the –24V output is not directly regulated, it still measures 2% from a 1mA to 7mA load.

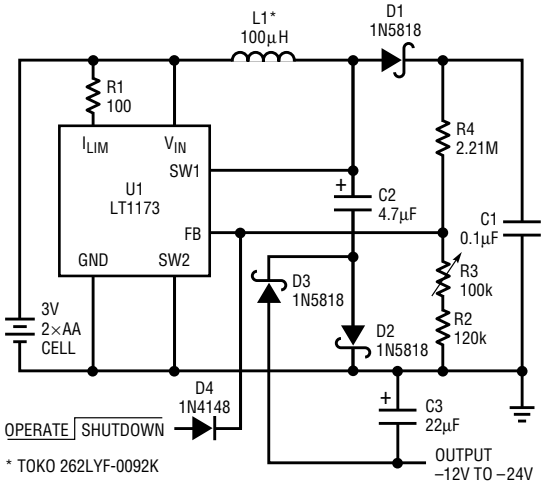


Figure 6. LCD bias generator (3V to -12 to -24V)

The circuit will deliver 7mA from a 2.0V input at 75% efficiency.

If greater output power is required, Figure 6's circuit can be driven from a +5V source. R1 should be changed to 47Ω and C3 to 47µF. With a 5V input, 40mA is available at 75% efficiency. Shutdown is accomplished by bringing the anode of D4 to a logic high, forcing the feedback pin of U1 to go above the internal 1.25V reference voltage. Shutdown current is 110µA from the input source and 36µA from the shutdown signal.

Another interesting modification of a boost converter that can provide negative bias from a 5V supply is shown in Figure 7. The converter, developed by Jon Dutra of LTC, is half switcher and half charge pump. The charge pump (C1, C2, D2, and D3) is driven by the flying node at V_{SW}. The output is variable from –10 to –30V, providing contrast control for the display.

On low-voltage supplies (6V or less) V_{IN} and V_{BATT} can be tied together. With higher battery voltages, high efficiency is obtained by running the LT1172 V_{IN} pin from 5V. Shutting off the 5V supply will automatically turn off the LT1172. The maximum value for V_{BATT} is equal to the negative output plus 1V. Also, the difference between V_{BATT} and V_{IN} must not exceed 16V. R1, R2, and R3 are made large to minimize battery drain in shutdown, since they are permanently connected to the battery via L1 and D1. Efficiency is about 80% at I_{OUT} = 25mA. LT

This article was extracted from LTC Application Note 49 available in August. For more details, and additional information, please request AN49 on the response card or call the 800 number listed on the last page of this magazine.

Laser Driver, continued from page 4

When power is applied, laser current is zero and A1's output goes to ground. The high-voltage converter supplies full output (3.5kV), but the laser does not start. Under these conditions, the C106 SCR is off and C2 charges. A divided-down portion of C2's voltage biases A1's positive input. When C2 reaches about 200V, A1's output goes high, triggering the SCR. This dumps C2's charge through L3 to ground. L3's output, a very-high-voltage spike, ionizes the laser, driving it into conduction. Laser impedance drops and the main current control loop begins behaving as described above. The presence of voltage across the 340Ω shunt causes A1's output to go low, preventing further SCR conduction. Zener clamp Z1 limits C2's voltage under these conditions. If the laser fails to start, the cycle will repeat until start-up occurs. Electrical efficiency for this circuit is about 75% for inputs from 22 to 35V. LT

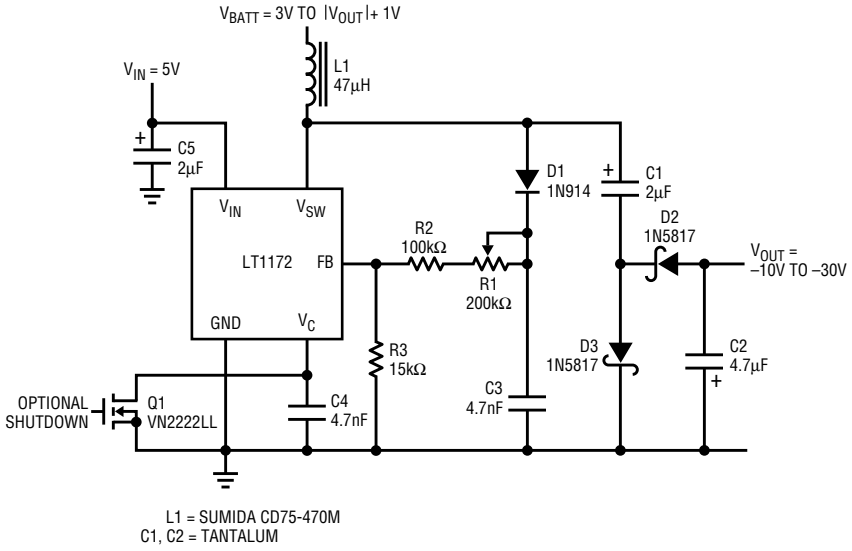


Figure 7. 5V LCD bias generator (5V to -10 to -30V)

[1] Don't say we didn't warn you!

[2] The term "efficiency" as used here refers to *electrical* efficiency. In fact, the ultimate concern centers around the efficient conversion of power-supply energy into light. Unfortunately, lamp types show considerable variation in their current-to-light conversion efficiency. Similarly, the emitted light for a given current varies over the life of any particular lamp. Hence, this article treats "efficiency" on an electrical basis: as the ratio of power removed from the primary supply to the power delivered to the lamp. When a lamp has been selected, this ratio can be measured with a photometer.

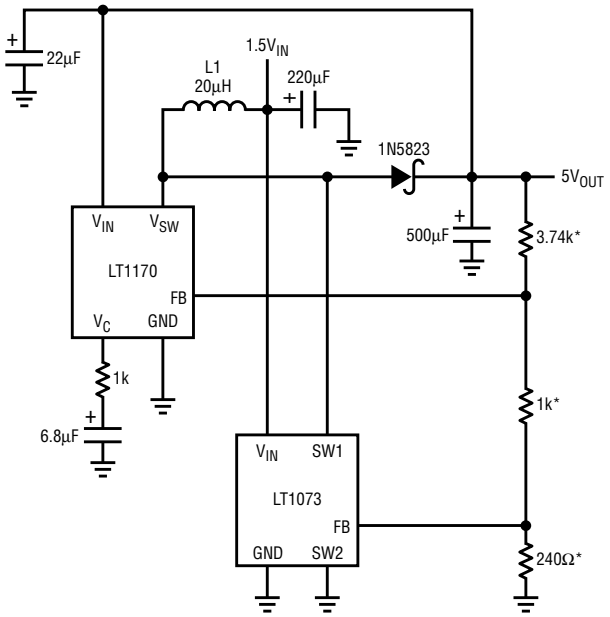
[3] The discontinuous energy delivery to the loop causes substantial jitter in the burst-repetition rate, although the high-voltage section maintains resonance. Unfortunately, circuit operation is in the "chop" region of most oscilloscopes, precluding a detailed display. "Alternate" operation causes waveform-phasing errors, also producing an inaccurate display. Hence, waveform observation requires special techniques. Figure 5 was taken with a dual-beam instrument (Tektronix 556) with both beams slaved to one time base. Single-sweep triggering eliminated jitter artifacts. Most 'scopes, whether analog or digital, will have trouble reproducing this display.

200mA Output, 1.5V-to-5V Converter

by Jim Williams

Some 1.5V powered systems, such as two-way survival radios, remote, transducer-fed data-acquisition systems, and the like, require much more power than stand-alone IC regulators can provide. Figure 1's design supplies a 5V output with 200mA capacity.

The circuit is essentially a flyback regulator. The LT1170 switching regulator's low saturation losses and ease of use permit high power operation and design simplicity. Unfortunately this device has a 3V minimum supply requirement. Bootstrapping its supply pin from the 5V output is possible, but requires some form of start-up mechanism. The 1.5V powered LT1073 switching regulator forms a start-up loop. When power is applied, the LT1073 starts, causing its V_{SW} pin to periodically pull current through L1. L1 responds with high-voltage flyback pulses. These pulses are rectified and stored in the 500µF capacitor, producing the circuit's DC output. The output-divider string is set up so the LT1073 turns off when the circuit's output crosses about 4.5V. Under these conditions the LT1073 can no longer drive L1, but the LT1170 can. When the start-up circuit turns off, the LT1170 V_{IN} pin has adequate supply voltage and it can operate. There is some overlap between start-up loop turn-off and LT1170 turn-on, but this has no detrimental effect. The start-up loop must function over a wide range of loads and battery voltages. Start-up currents are about 1 ampere, necessitating attention to the LT1073's saturation and drive characteristics. The worst case is a nearly depleted battery and heavy output loading. Figure 2 plots input/output characteristics for the circuit. Note that the circuit will start into all loads with V_{BATT} = 1.2V. Start-up is possible down to 1.0V at reduced loads. Once the circuit has started, the plot shows it will drive full 200mA loads down to V_{BATT} = 0.6V (a very dead battery). Figure 3 graphs efficiency at two supply voltages over a range of output currents. Performance is attractive, although at lower currents circuit quiescent power degrades efficiency. Fixed junction saturation losses are responsible for lower overall efficiency at the lower supply voltage.



L1 = COILTRONICS CTX20-5-52, COILTRONICS (305) 781-8900
* = 1% METAL FILM RESISTOR

Figure 1. 200mA output, 1.5V-to-5V converter

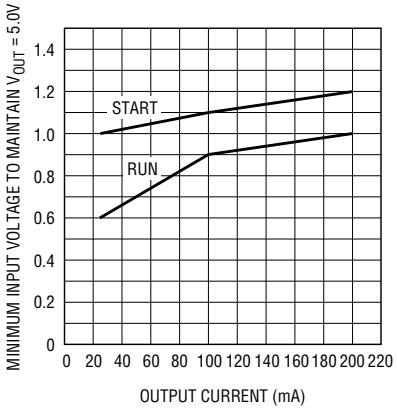


Figure 2. Input/output data for Figure 1

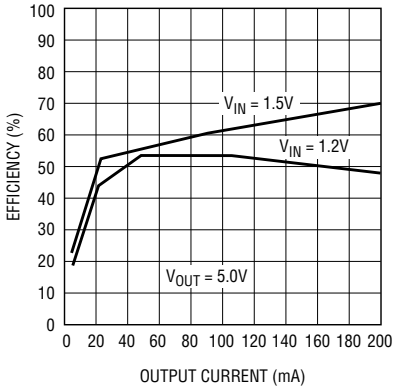


Figure 3. Efficiency versus operating point for Figure 1

References

1. Williams, Jim and Brian Huffman. "Some Thoughts on DC–DC converters", pages 13–17, "1.5V to 5V Converters." Linear Technology Corporation Application Note 29, October 1988.

A Simple, Efficient Laser Power Supply

by Jim Williams

Helium-neon lasers, used for a variety of tasks, are difficult loads for a power supply. They typically need almost 10 kilovolts to start conduction, although they require about 1500 volts to maintain conduction at their specified operating currents. Powering a laser usually involves some form of start-up circuitry to generate the initial breakdown voltage and a separate supply for sustaining conduction. Figure 1's circuit considerably simplifies driving the laser. The start-up and sustaining functions have been combined into a single, closed-loop current source with over 10 kilovolts of compliance. When power is applied, the laser does not conduct and the voltage across the 190Ω resistor is zero. The LT1170 switching regulator FB pin sees no feedback voltage, and its switch pin (V_{SW}) provides full duty cycle pulse-width modulation to L2. Current flows from L1's center tap through Q1 and Q2 into L2 and the LT1170. This current flow causes Q1 and Q2 to switch, alternately driving L1. The 0.47µF capacitor resonates with L1, providing a boosted, sine-wave drive. L1 provides substantial step-up, causing about 3500 volts to appear at its secondary. The capacitors and diodes associated with L1's secondary form a voltage tripler, producing over 10 kilovolts across the laser. The laser breaks down and current begins to flow through it. The 47kΩ resistor limits current and isolates the laser's load characteristic. The current flow causes a voltage to appear across the 190Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin, closing a control loop. The LT1170 adjusts its pulse-width drive to L2 to maintain the FB pin at 1.23 volts, regardless of changes in operating conditions. Hence, the laser sees constant current drive, in this case 6.5mA. Other currents are obtainable by varying the 190Ω value. The IN4002 diode string clamps excessive voltages when laser conduction first begins, protecting the LT1170. The 10µF capacitor at the V_C pin frequency compensates the loop and the MUR405 maintains L1's current flow when the LT1170 V_{SW} pin is not conducting. The circuit will start and run the laser over a 9–35 volt input range with an electrical efficiency of about 75%. LT

References

1. Williams, Jim. "Illumination Circuitry for Liquid Crystal Displays" Linear Technology Application Note 49, August 1992.

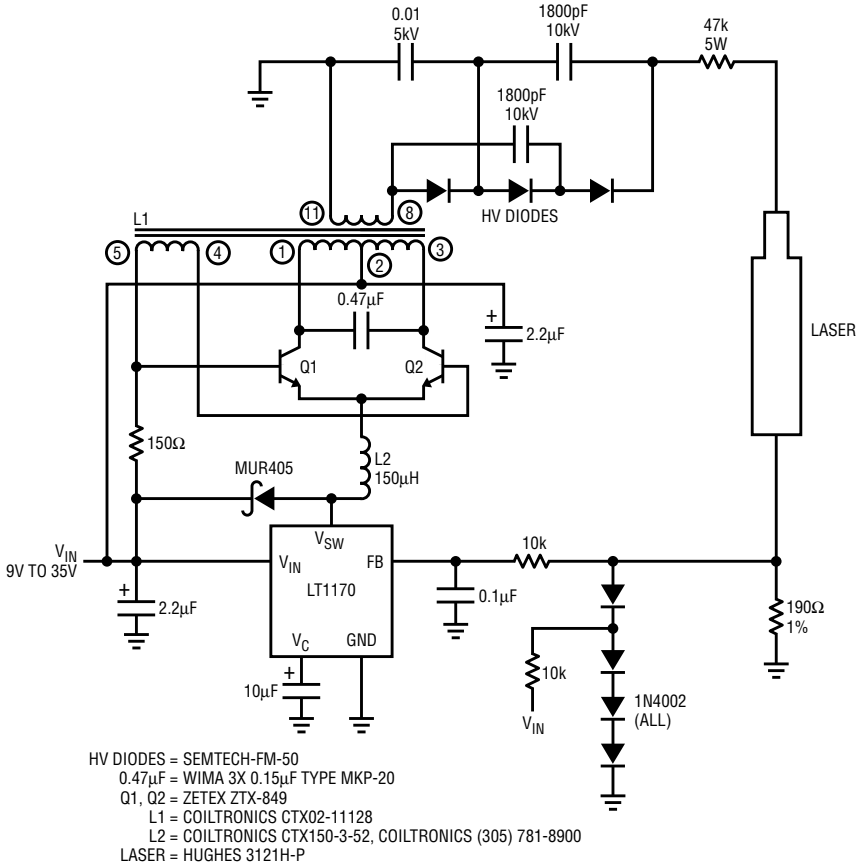


Figure 1. Laser power supply

Noise Generators for Multiple Uses

A Broadband Random Noise Generator

by Jim Williams

Filter, audio, and RF-communications testing often require a random noise source. Figure 1's circuit provides an RMS-amplitude regulated noise source with selectable bandwidth. RMS output is 300 millivolts, with a 1kHz to 5MHz bandwidth, selectable in decade ranges.

Noise source D1 is AC coupled to A2, which provides a broadband gain of 100. A2's output feeds a gain-control stage via a simple, selectable lowpass filter. The filter's output is applied to A3, an LT1228 operational transconductance amplifier. A1's output feeds LT1228 A4, a current-feedback amplifier. A4's output, which is also the circuit's output, is sampled by the A5-based gain-control configuration. This closes a gain control loop to A3. A3's I_{SET} current controls gain, allowing overall output level control.

Figure 2 plots noise at a 1MHz bandpass, whereas Figure 3 shows RMS noise versus frequency in the same bandpass. Figure 4 plots similar information at full bandwidth (5MHz). RMS output is essentially flat to 1.5MHz, with about ±2dB control to 5MHz before sagging badly.

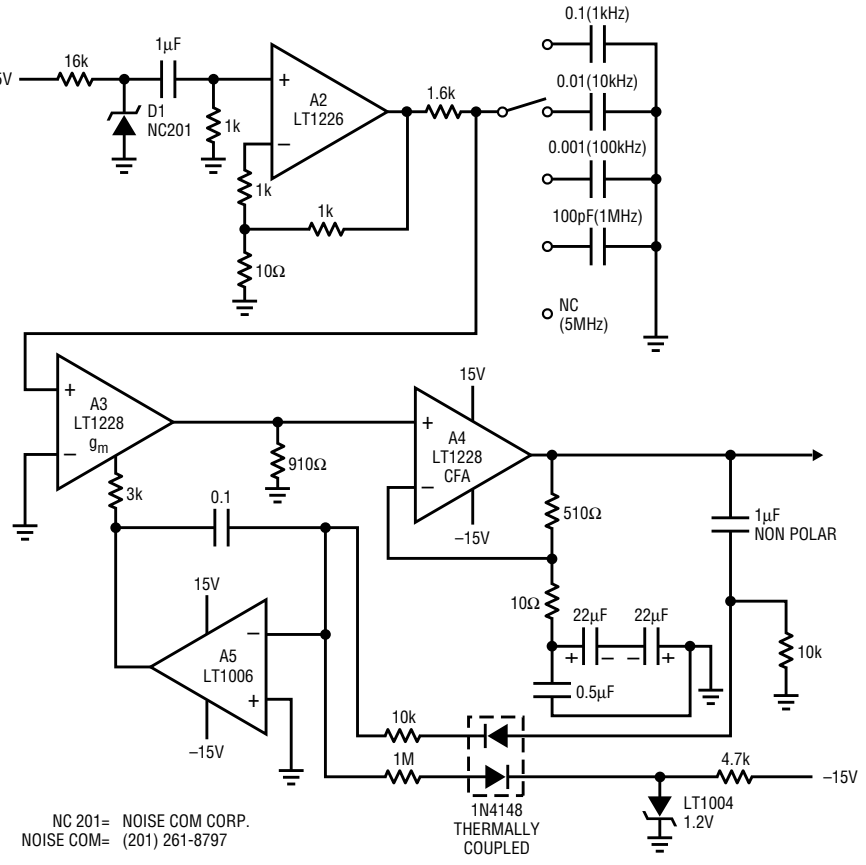


Figure 1. Broadband random noise generator schematic

A Diode Noise Generator for "Eye Diagram" Testing

by Richard Markell

The circuit that Jim Williams describes evolved from my desire to build a circuit for testing communications channels by means of "eye diagrams." (See *Linear Technology*, Volume I, Number 2 for a short explanation of the eye diagram.) I wanted to replace my pseudo-random code generator circuit, which used a PROM, with a more "analog" design—one that more people could build without specialized components. What evolved was a noise source sampled by a very fast comparator (see Figure 5). The comparator outputs a random pattern of 1's and 0's.

The noise diode (an NC201) is filtered and amplified by the LT1190 high-speed operational amplifier (U1). The output feeds the LT1116 (U2), a 12ns, single-supply, ground-sensing comparator. The 2kΩ pot at the inverting input of the LT1116 sets the threshold to the comparator so that a quasi-equal number of 1's and 0's are output. U3 latches the output from U2 so that the output from the comparator remains latched throughout one clock period. The two-level output is taken from U3's Q0 output.

The additional circuitry shown in the schematic diagram allows the circuit to output four-level data for PAM (pulse amplitude modulation) testing. The random data from the two-level output is input to a shift register, which is reset on every fourth clock pulse. The output from the shift register is weighted by the three 5kΩ resistors and summed into the LT1220 operational amplifier from which the output is taken. The filter network between the 74HC74 output and the 74HC4094 strobe input is necessary to ensure that the output data is correct.

Clock-Synchronized Switching Regulator has Coherent Noise

by Jim Williams, Sean Gold, and Steve Pietkiewicz

Gated-oscillator-type switching regulators permit high efficiency over extended ranges of output current. These regulators achieve this desirable characteristic by using a gated-oscillator architecture instead of a clocked pulse-width modulator. This eliminates the "housekeeping" currents associated with the continuous operation of fixed-frequency designs. Gated-oscillator regulators simply self-clock at whatever frequency is required to maintain the output voltage. Typically, loop-oscillation frequency ranges from a few hertz into the kilohertz region, depending upon the load.

This asynchronous, variable frequency operation seldom creates problems; some systems, however, are sensitive to this characteristic. The circuit in Figure 1 slightly modifies a gated-oscillator-type switching regulator by synchronizing its loop-oscillation frequency to the system's clock. In this fashion the oscillation frequency and its attendant switching noise, although variable, are made coherent with system operation.

Circuit operation is best understood by temporarily ignoring the flip-flop and assuming that the LT1107 regulator's A_{OUT} and FB pins are connected. When the output voltage decays, the set pin drops below V_{REF}, causing A_{OUT} to fall. This causes the internal comparator to switch high, biasing the oscillator and output transistor into conduction. L1 receives pulsed drive, and its flyback events are deposited into the 100µF capacitor via the diode, restoring output voltage. This overdrives the set pin, causing the IC to switch off until another cycle is required.

The frequency of this oscillatory cycle is load dependent and variable. If a flip-flop is interposed in the A_{OUT}–FB pin path, as shown, the frequency is synchronized to the system clock. When the output decays far enough (trace A, Figure 2) the A_{OUT} pin (trace B) goes low. At the next clock pulse (trace C) the flip-flop Q2 output (trace D) sets low, biasing the comparator-oscillator. This turns on the power switch (V_{SW} pin is trace E), which pulses L1. L1 responds in flyback fashion, depositing its energy into the output capacitor to maintain

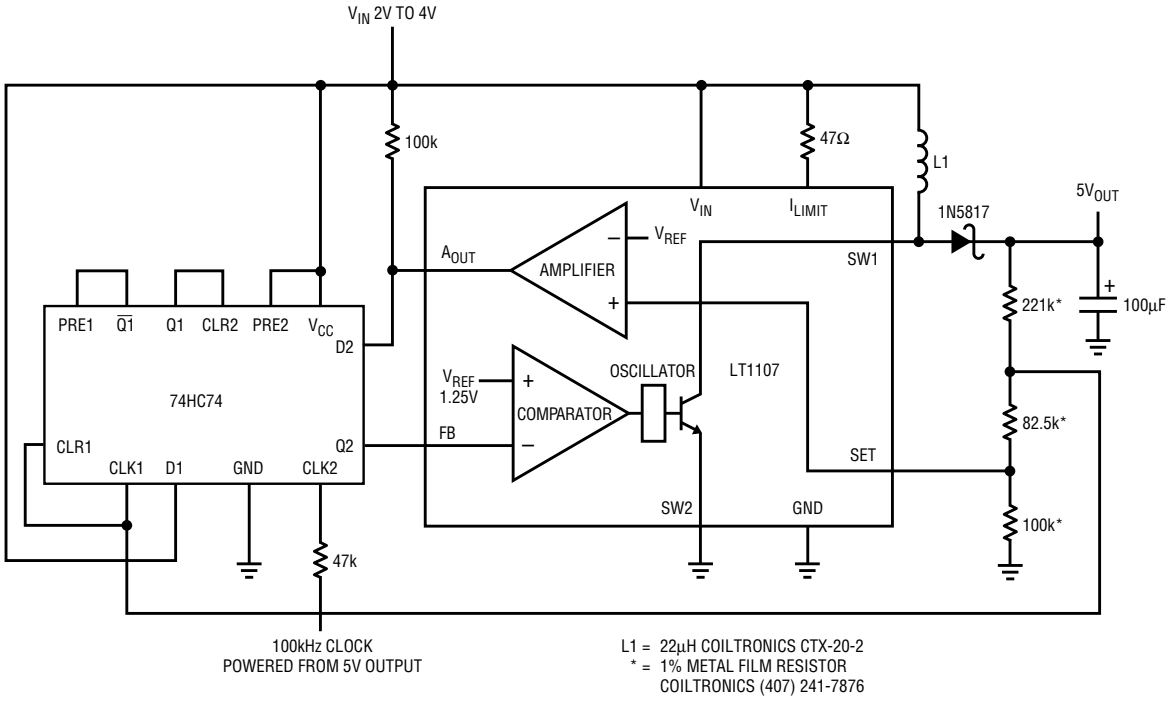


Figure 1. A synchronizing flip-flop forces switching regulator noise to be coherent with the clock

output voltage. This operation is similar to the previously described case, except that the sequence is forced to synchronize with the system clock by the flip-flop's action. Although the resulting loop's oscillation frequency is variable, it, and all its attendant switching noise, are synchronous and coherent with the system clock.

Because of its sampled nature, this clocked loop may not start. To ensure start-up, the flip-flop's remaining section is connected as a buffer. The CLR1–CLK1 line monitors output voltage via the resistor string. If the circuit does not start, Q1 is asserted, CLR2 sets, and loop operation commences. Although the circuit shown is a step-up type, any switching regulator configuration can use this technique. LT

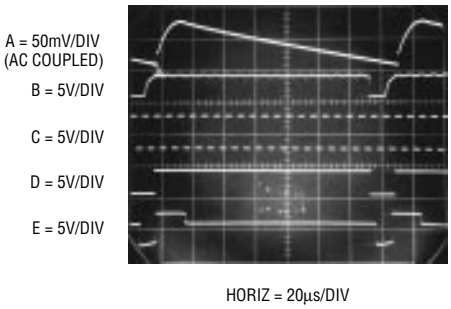


Figure 2. Waveforms for the clock-synchronized switching regulator. The regulator switches (trace E) only on clock transitions (trace C), resulting in clock-coherent output noise (trace A)

An Isolated High-Side Driver

by James Herr

Introduction

The LTC1146 low-power digital isolator draws only 70µA of supply current with V_{IN} = 5V. Its low supply current feature is well suited for battery-powered systems that require isolation, such as an isolated high-side driver. The LTC1146A is rated at 2500V_{RMS} and is UL approved. The LTC1146 is intended for less stringent applications. It is rated at 500VDC.

Theory of Operation

Opto-isolators available today require supply currents in the milliampere range even for low-speed operation (less than 20kHz). This high supply current is another drain on the battery. Figure 1 shows the alternative of using an LTC1146A to drive an external power MOSFET (IRF840) at speeds to 20kHz with V+ = 300V.

The input pin of LTC1146A must be driven with a signal that swings at least 3 volts (referred to GND1, which is a floating ground). The O_S pin outputs a square wave corresponding to the input signal, but with a time delay. The amplitude of the output square wave is equal to the potential at the V_{CC} pin. The TL4426 is a high-speed MOSFET driver used here to supply gate-drive current to the power MOSFET. The power supply to the LTC1146A and the TL4426 is bootstrapped from a 13V supply referred to system ground. C1 supplies the current to both the LTC1146A and the TL4426 when the power MOSFET is being turned on. Its value should be increased when the input signal's ON time increases. D3 prevents the output from swinging negative due to stray inductance. If the output goes below ground, the gate-to-source voltage of the IRF840 rises. This high potential could damage the power MOSFET. The output slew rate should be limited to 1000V/µs to prevent glitches on the O_S output of the LTC1146A. LT

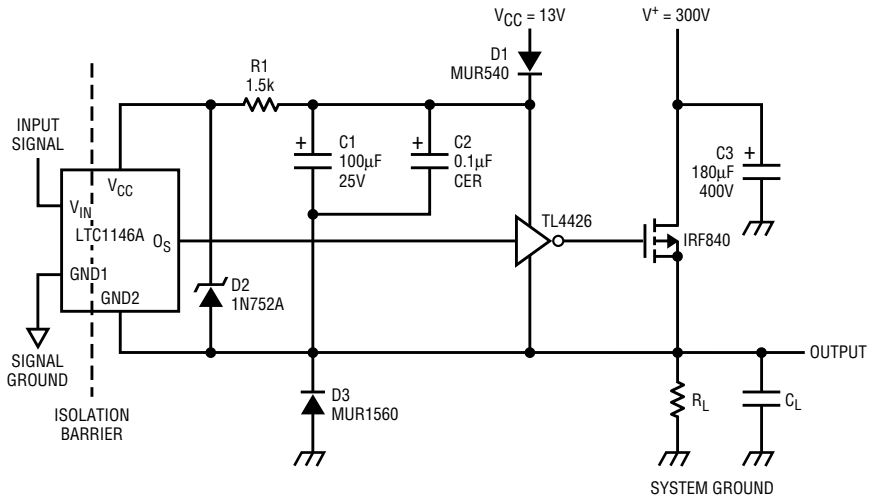


Figure 1. Isolated high-side driver schematic diagram

A Single-Cell Barometer

by Jim Williams and
Steve Pietkiewicz

Figure 1, a complete barometric pressure signal conditioner, operates from a single 1.5V battery. Until recently, high accuracy and stability have been obtainable only with bonded strain gage and capacitively based transducers, which are quite expensive. This design, using a recently introduced semiconductor transducer, achieves .01"Hg (inches of mercury) uncertainty over time and temperature. The 1.5V powered operation permits portable application.

The 6kΩ transducer (T1) requires precisely 1.5mA of excitation, necessitating a relatively high voltage drive. A1's positive input senses T1's current by monitoring the voltage drop across the resistor string in T1's return path. A1's negative input is fixed by the 1.2V LT1004 reference. A1's output biases the 1.5V powered LT1110 switching regulator. The LT1110's switching produces two outputs from L1. Pin 4's rectified and filtered output powers A1 and T1. A1's output, in turn, closes a feedback loop at the regulator. This loop generates whatever voltage step-up is required to force precisely 1.5mA through T1. This arrangement provides the required high-voltage drive while minimizing power consumption. This occurs because the switching regulator produces only enough voltage to satisfy T1's current requirements.

L1 pins 1 and 2 source a boosted, fully floating voltage, which is rectified and filtered. This potential powers A2. Because A2 floats with respect to T1, it can look differentially across T1's outputs, pins 10 and 4. In practice, pin 10 becomes "ground" and A2 measures pin 4's output with respect to this point. A2's gain-scaled output is the circuit's output, conveniently scaled at 3.000V = 30.00"Hg.

To calibrate the circuit, adjust R1 for 150mV across the 100Ω resistor in T1's return path. This sets T1's current to the manufacturer's specified calibration point. Next, adjust R2 at a scale factor of 3.000V = 30.00"Hg. If R2 cannot capture the calibration, reselect the 200kΩ resistor in series with it. If a pressure standard is not available, the transducer is supplied with individual calibration data, permitting circuit calibration.

This circuit, compared to a high-order pressure standard, maintained .01"Hg accuracy over months with widely varying ambient pressure shifts. Changes in pressure, particularly rapid ones, correlated quite nicely to changing weather conditions. Additionally, because .01"Hg corresponds to about 10 feet of altitude at sea level, driving over hills and freeway overpasses becomes quite interesting. The circuit pulls 14mA from the battery, allowing about 250 hours operation from one D cell.

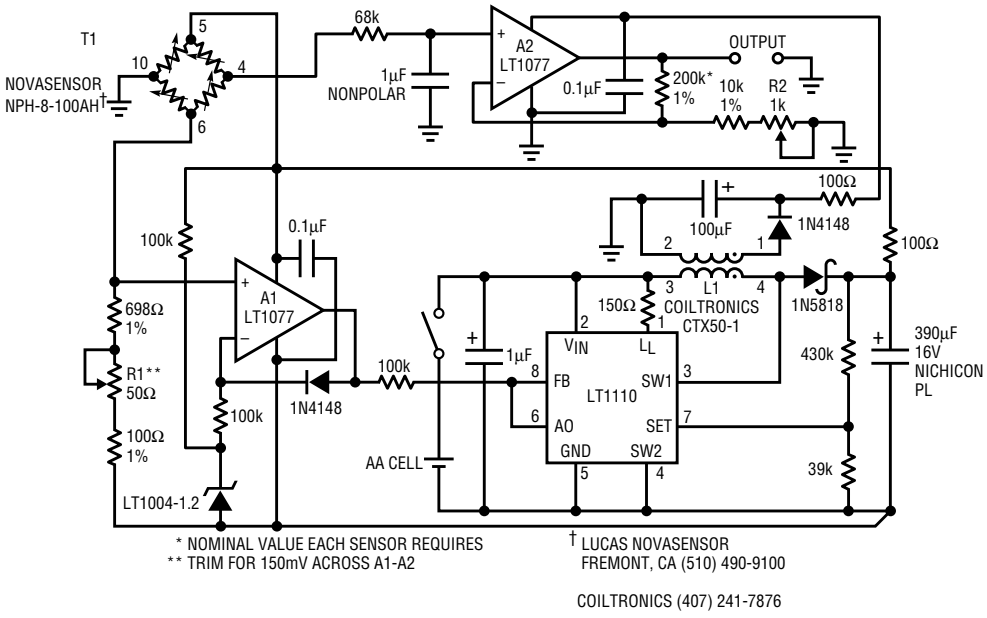


Figure 1. Schematic diagram: single-cell barometer

Selection Criteria for CCFL Circuits

by Jim Williams

Previous LTC publications have discussed issues and circuitry related to powering cold cathode fluorescent lamps (CCFLs).[1] These lamps are almost universally employed for backlighting liquid crystal displays (LCDs). The large variety of displays and applications necessitates a wide range of circuit approaches. A single method providing optimal results in all situations, although desirable, remains elusive. As a result, a very wide array of potential solutions have been developed and presented. This makes selecting an approach for any given application somewhat confusing.

Comfort arrives with the realization that the circuits fall into two broad categories. All approaches drive the lamp in either a "grounded" or "floating" configuration. Understanding these terms and their significance in selecting a lamp-driving approach is the subject of this tutorial.

Sources of Energy Loss in Practical Applications

Achieving high efficiency for a backlight design requires careful attention to the physical layout of the lamp, its leads and the construction of the display housing. Parasitic capacitance from any high voltage point to DC or AC ground creates a path for unwanted current flow. This parasitic current degrades electrical efficiency. The loss term is related to $1/2CV^2f$ where C is the parasitic capacitance, V is the voltage at any point on the lamp and f is the operating frequency. Losses up to 25% have been observed. Layout techniques that increase parasitic capacitance include long high voltage lamp leads, reflective metal foil around the lamp and displays supplied in metal enclosures.

Grounded circuits drive the lamp in single-ended fashion. Figure 1 shows one lamp electrode receiving drive with the other terminal essentially at ground. This causes significant loss via parasitic paths associated with the lamp's driven end.

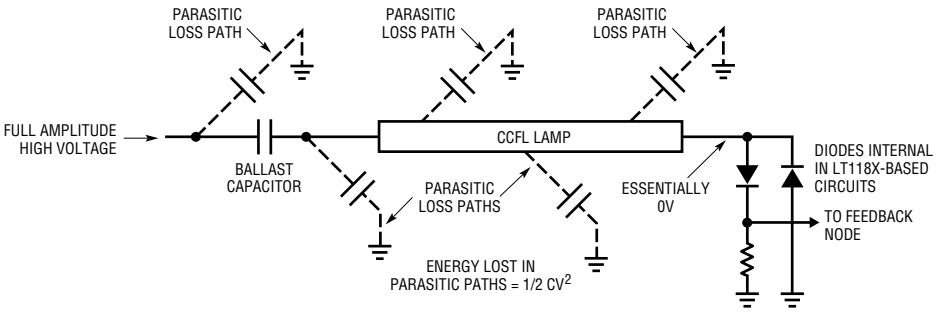


Figure 1. Ground-referred lamp drive has large energy loss in high voltage regions due to full amplitude swing.

This is so because of the large voltage swing in this region. The parasitic paths near the lamp's grounded end undergo relatively little swing, contributing small energy loss. Unfortunately, the lost energy is heavily voltage dependent ($E = 1/2CV^2$) and net energy loss is excessive if driven-end parasitics are large. Figure 2's configuration minimizes the losses by altering the drive scheme. In this case the lamp is driven from both ends instead of one end being grounded.

This "floating" lamp arrangement requires only half the voltage swing at each end instead of full swing at one end. This introduces more loss in the parasitic paths previously tied to the grounded end. In most cases, these increased losses are favorably offset by the reduced swing because of the V^2 loss term associated with voltage amplitude.

The advantage gained varies considerably with display type, although a 10% to 20% reduction in lost energy is common. In some displays loss reduction is not as good, and occasionally the improvement is negligible. Heavily asymmetric wiring to or within the display can sometimes make floating drive more lossy than grounded drive. In such cases, testing in both modes is necessary to determine which type of drive is most efficient.

A second advantage of floating operation is extended illumination range. Grounded lamps operating at relatively low currents may display the "thermometer effect"; that is, light intensity may be nonuniformly distributed along the lamp's length.

Figure 3's grounded scheme shows that although lamp-current density is uniform, the associated field is imbalanced. The field's low intensity, combined with its imbalance, means

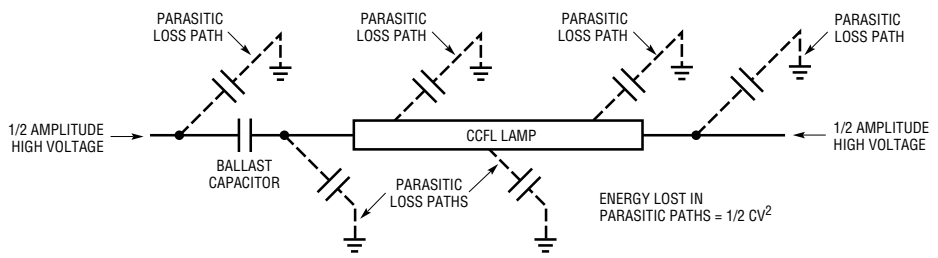


Figure 2. "Floating" lamp allows reduced bipolar drive, cutting losses due to parasitic capacitance paths. Formerly grounded lamp end's paths absorb more energy than before, but overall loss is lower due to equation's V^2 term.

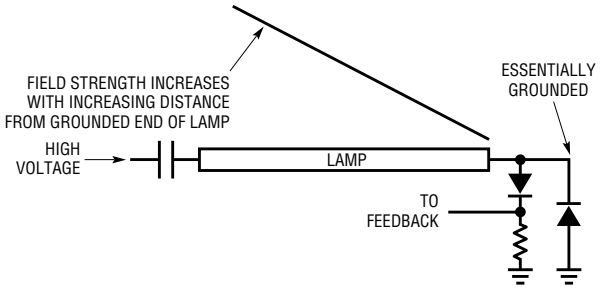


Figure 3. Field strength versus distance for a ground referred lamp. Field imbalance promotes uneven illumination at low drive levels.

that there is not enough energy to maintain uniform phosphor glow beyond some point. Lamps displaying the thermometer effect emit most of their light near the driven electrode, with rapid emission fall-off as distance from the electrode increases.

Some displays require extended illumination range. "Thermometering" usually limits the lowest practical illumination level. One acceptable way to minimize thermometering is to eliminate the large field imbalance. The floating drive used to reduce energy loss also provides a way to minimize thermometering.

Figure 4 shows the effects of floating drive on lamp-field balance. The balanced field provides excitation at both lamp ends, aiding low current illumination. In a well optimized floating-lamp display, thermometering starts in the lamp's center, simultaneously proceeding towards both ends as drive is reduced.

Selection Criteria

The different characteristics of grounded and floating circuits should be kept in focus when reviewing a particular application's requirements.

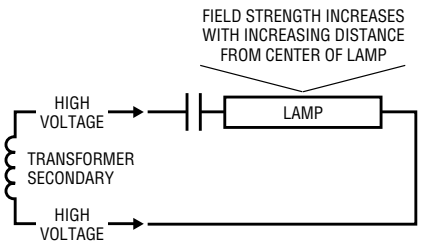


Figure 4. Field strength versus distance for a floating lamp. Improving field imbalance permits extended illumination range at low levels.

Selecting which CCFL circuit to use for a specific application involves numerous trade-offs. A variety of issues determine which circuit is the "best" approach. At a minimum, the user should consider the following guidelines before committing to any approach.

Display Characteristics

The display characteristics (including wiring losses) should be well understood. Typically, display manufacturers list lamp requirements. These specifications are often obtained from the lamp vendor, who usually tests in free air, with no significant parasitic loss paths. This means that the actual required power, start and running voltages may differ significantly from the datasheet specifications. The only way to be certain of display characteristics is to measure them. The measured display energy loss can determine whether a floating or grounded circuit is applicable. Low loss displays (relatively rare) usually provide better overall efficiency with grounded drive. As losses become worse (unfortunately, relatively common) floating drive becomes a better choice. Efficiency measurements in both modes may be required to determine the best choice.

Operating Voltage Range

The operating voltage range spans the minimum and maximum voltages from which the circuit must operate. In battery-driven apparatus, the supply range can easily be 3:1 or greater. The best backlight performance is usually obtained in the 8V–28V range. In general, potentials below 7V require some efficiency trade-offs at moderate (1.5W to 3W) power levels. Some systems reduce backlight power when running from the battery, and this can have a pronounced effect on the design. Even seemingly small (e.g., 20%) reductions in power may eliminate painful trade-offs. In particular, high-turns-ratio transformers are required to support low voltage operation at full lamp output. These transformers work well, but are somewhat less efficient than those with lower turns ratios, due to their higher characteristic peak currents. Prevailing trends in battery technology encourage system operation at low voltages, necessitating extreme care in transformer selection and Royer circuit design.

Auxiliary Operating Voltages

Auxiliary logic supply voltages should be used (if available) to run CCFL "housekeeping" currents, such as IC V_{IN} pins. This saves power. Always run switching regulators from the lowest potential available, usually 3.3V or 5V. Many systems provide these voltages in switched form, making separate shutdown lines unnecessary. Turning off the switching regulator's supply shuts down the entire backlight circuit.

Line Regulation

Grounded lamp circuits, by virtue of their true global feedback, provide the best line regulation. For abrupt changes, a user may notice anything beyond a 1% variation in regulation. A grounded circuit easily meets this requirement; a floating circuit will usually do so. Excursions beyond 1%, caused by slowly changing line inputs, are not normally a problem because they are not detectable. Rapid line changes, such as plugging in a system AC line adapter, require good regulation to avoid annoying display flicker.

Power Requirements

The CCFL's power requirement, *including display and wiring losses*, should be well defined over all condi-

Table 1. Characteristics of LT parts families

Issues	LT118X Series	LT117X Series	LT137X Series
Optical Efficiency	Grounded output versions display dependent. Floating versions usually 5% to 20% better	Display dependent	Display dependent
Electrical Efficiency	Grounded output versions—75% to 90%, depending on supply voltage and display. Floating output versions slightly lower	75% to 90%, depending on supply voltage and display	75% to 92%, depending on supply voltage and display
Lamp Current Certainty	1% to 2% for grounded versions, 1% to 4% for floating output types	2% maximum	2% maximum
Line Regulation	0.1% to 0.3% for grounded types, 0.5% to 6% for floating versions	0.1% to 0.3%	0.1% to 3%
Operating Voltage Range	5.3V to 30V, depending on output power, temperature range, display, etc.	4.0V to 30V, depending on output power, temperature range, display, etc.	4.0V to 30V, depending on output power, temperature range, display, etc.
Power Range	0.75W to 6W typical	0.75W to 20W typical	0.5W to 6W typical
Supply Current Profile	Continuous— no high current peaks	Continuous— no high current peaks	Continuous— no high current peaks
Shutdown Control	Yes—logic compatible	Requires small FET or bipolar transistor	Yes—logic compatible
Transient Response—Overshoot	Excellent— no optimization required	Excellent—requires optimization in some cases	Excellent—requires optimization in some cases
Dimming Control	Pot., PWM, variable DC voltage or current. LT1186 has serial digital input with data storage.	Pot., PWM, variable DC voltage or current	Pot., PWM, variable DC voltage or current
Emissions	Low	Low	Low, although high power versions may require attention tolayout and shielding
Open Lamp Protection	Internal to IC	Requires external small-signal transistor and some discretes at high supply voltages	Requires external small-signal transistor and some discretes at high supply voltages
Size	Low component count, small overall board footprint. 200kHz magnetics.	Small—100kHz magnetics	Small—1MHz magnetics for fastest versions
Contrast Supply Capability	Various contrast supply options available, including bipolar output	No	No

tions, including temperature and lamp-specification variations. Usually, IC versions of floating lamp circuits are restricted to 3W to 4W output power, whereas grounded-circuit power is easily scaled.

Supply Current Profile

The backlight is often located far "forward" in the system. Impedance in cables, switches, traces and connectors can build up to significant levels. This means that a CCFL circuit should draw operating power continuously, rather than requiring discrete, high current "chunks" from a lossy supply line. Royer-based architectures are nearly ideal in this regard, pulling current smoothly over time and requiring no special bypassing, supply impedance or layout treatment. Similarly, Royer-type circuits do not cause significant disturbances to the supply line, preventing noise injection back into the supply.

Lamp Current Certainty

Lamp current accuracy at full intensity is important for maintaining lamp life. Excessive overcurrent greatly shortens lamp life, while yielding little luminosity benefit. Grounded circuits are excellent in this category, with 1% accuracy usually achieved. Floating circuits are typically in the 2% range. Tight current tolerances do not benefit unit/unit display luminosity because lamp emission and

Table 1. (continued)

Issues	LT1269/LT1270	LT1301	LT1173
Optical Efficiency	Display dependent	Display dependent	Display dependent
Electrical Efficiency	75% to 90%, depending on supply voltage and display	70% to 88%, depending on supply voltage and display	65% to 75%, depending on supply voltage and display
Lamp Current Certainty	2% maximum	2% typical	5%
Line Regulation	0.1% to 0.3%	0.1% to 0.3%	8% to 10%
Operating Voltage Range	4.5V to 30V, depending on output power, temperature range, display, etc.	2V to 10V practical	2V to 6V practical
Power Range	5W to 35W typical	0.02W to 1W practical	Essentially 0W to about 0.6W
Supply Current Profile	Continuous—no high current peaks	Continuous—no high current peaks	Irregular—relatively high current peaking requires attention to supply rail impedance
Shutdown Control	Requires small FET or bipolar transistor	Yes—logic compatible	Logic compatible shutdown practical
Transient Response—Overshoot	Excellent—requires optimization in some cases	Excellent—no optimization required	Excellent—no optimization required
Dimming Control	Pot., PWM, variable DC voltage or current	Pot., PWM, variable DC voltage or current	Pot., PWM, variable DC voltage or current
Emissions	High power mandates attention to layout and shielding	Very low	Itsy-bitsy
Open-Lamp Protection	Requires external small-signal transistor and some discretes at high supply voltages	Requires external small-signal tansistor and some discretes, but low supply voltages usually eliminate this consideration	None, but low supply, low power operation usually eliminates this issue
Size	Relatively large due to high power 100kHz magnetics	Very small—low power magnetics cut size	Small—low power magnetics cut size
Contrast Supply Capability	No	No	No

display attenuation variations approach ±20% and vary over life.

Efficiency

CCFL backlight efficiency should be considered from two perspectives. The electrical efficiency is the ability of the circuit to convert DC power to high voltage AC and deliver it to the load (lamp and parasitic) with minimum loss. The optical efficiency is perhaps more meaningful to the user. It is simply the ratio of display luminosity to DC power into the CCFL circuit. The electrical and optical losses are lumped together in this measurement to produce a luminosity versus power specification. It is quite significant that the electrical and optical peak efficiency operating points do not necessarily coincide. This is primarily due to the dependence of the lamp's emissivity on wave shape. The optimum wave shape for emissivity may or may not coincide with the circuit's electrical operating peak. In fact, it is quite possible for inefficient circuits to produce more light than more efficient versions. The only way to ensure peak efficiency in a given situation is to optimize the circuit to the display.

Shutdown

System shutdown almost always requires turning off the backlight. In many cases, the low voltage supply is already available in switched form. If this is so, the CCFL circuits turn off, absorbing very little power. If switched low voltage power is not available, the shutdown inputs may be used, requiring an extra control line.

Transient Response

The CCFL circuit should turn on the lamp without attendant overshoot or poor control loop settling characteristics. This can cause objectionable display flicker, and, in the worst case, result in transformer overstress and failure. Properly prepared floating and grounded CCFL circuits have good transient response, with LT118X-based types being inherently easier to optimize.

Dimming Control

The method of dimming should be considered early in the design. All of the circuits shown in this article can be controlled by potentiometers, DC voltages and currents, pulse-width modulation or serial data protocols. Use a dimming scheme with high

Table 2. Features of LT118X series parts

Part	LT1182	LT1183	LT1184	LT1184F	LT1186
Floating-Lamp Operation	Yes	Yes	No	Yes	Yes
Grounded-Lamp Operation	Yes	Yes	Yes	Yes	Yes
Contrast Supply	Bipolar Contrast Outputs	Unipolar Contrast Outputs	No	No	No
Voltage Reference Available	No	Yes	Yes	Yes	No
Internal Control DAC	No	No	No	No	Yes

accuracy at maximum current to prevent excessive lamp drive.

Open Lamp Protection

The CCFL circuits deliver a current source output. If the lamp is broken or disconnected, the compliance voltage is limited by the transformer turns ratio and DC input voltage. Excessive voltage can cause arcing and resultant damage. Typically, the transformers withstand this condition, but open lamp protection will ensure against failures. This feature is built into the LT118X series; it must be added to other circuits.

Size

Backlight circuits usually have severe size and component-count limitations. The board must fit within tightly defined dimensions. LT118X series-based circuits offer the lowest component count, although board space is usually dominated by the Royer transformer. In extremely tight spaces, it may be necessary to physically segment the circuit, but this should be considered only as a last resort.

Contrast Supply Capability

Some LT118X parts provide contrast-supply outputs. The other circuits do not. The LT118X's onboard contrast supply is usually an advantage, but space is sometimes so restricted that it cannot be used. In such cases the contrast supply must be remotely located.

Emissions

Backlight circuits rarely cause emission problems, and shielding is usually not required. Higher power versions (for example, above 5W) may require attention to meet emission requirements. The fast-rise switching regulator output sometimes causes more RFI than the high voltage AC waveform. If shielding is used, its parasitic effects are part of the inverter load and optimization must be carried out with the shield in place.

Summary of Circuits

The interdependence of backlight parameters makes summarizing or rating various approaches a hazardous exercise. There is simply no intellectually responsible way to streamline the selection and design process if optimum results are desired. A meaningful choice *must* be the outcome of laboratory-based experimentation. There are just too many interdependent variables and surprises for a systematic, theoretically based selection. Pure analytics are pretty—working circuits come from the bench. Some generalizations of limited use are, however, possible. Tables 1 and 2 attempt to summarize salient characteristics versus part type and may (however cautiously) be considered as a beginning point. [2]

Table1 summarizes characteristics of all the circuits. Table 2 focuses on the features of the LT118X series parts. LT

References:

1. Williams, Jim. *Measurement and Control Circuit Collection.* Linear Technology Corporation Application Note 45, June 1991.
2. Williams, Jim. *Illumination Circuitry for Liquid Crystal Displays.* Linear Technology Corporation Application Note 49, August 1992.
3. Williams, Jim. *Techniques for 92% Efficient LCD Illumination.* Linear Technology Corporation Application Note 55, August 1993.
4. Bonte, Anthony. *LT1182 Floating CCFL with Dual Polarity Contrast.* Linear Technology Corporation Design Note 99, March 1995.
5. Williams, Jim. *A Fourth Generation of LCD Backlight Technology.* Linear Technology Corporation Application Note 65, December 1995.

Notes:

[1] LTC's investigation of CCFLs has been reported in a continuing series of publications, which appear in the "References" at the end of this article. In particular, reference 5 (the source of this text) reviews all previous work and presents recent findings.

[2] Readers detecting author ambivalence about the inclusion of Tables 1 and 2 are not hallucinating.

Authors can be contacted at (408) 432-1900

LTC1441-Based Micropower Voltage-to-Frequency Converter

by Jim Williams

Figure 1 is a voltage-to-frequency converter. A 0V–5V input produces a 0–10kHz output, with a linearity of 0.02%. Gain drift is 60ppm/°C. Maximum current consumption is only 26µA, 100 times lower than currently available units.

To understand the circuit's operation, assume that C1's negative input is slightly below its positive input (C2's output is low). The input voltage causes a positive-going ramp at C1's input (trace A, Figure 2). C1's output is high, allowing current flow from Q1's emitter, through C1's output stage to the 100pF capacitor. The 2.2µF capacitor provides high frequency bypass, maintaining low impedance at Q1's emitter. Diode connected Q6 provides a path to ground. The voltage to which the 100pF unit charges is a function of Q1's emitter potential and Q6's drop. C1's CMOS output, purely ohmic, contributes no voltage error. When the ramp at C1's negative input goes high enough, C1's output goes low (trace B) and the inverter switches high (trace C). This action pulls current from C1's negative input capacitor via the Q5 route (trace D). This current removal resets C1's negative input ramp to a potential slightly below ground. The 50pF capacitor furnishes AC positive feedback (C1's positive input is trace E) ensuring that C1's output remains negative long enough for a complete discharge of the 100pF capacitor. The Schottky diode prevents C1's input from being driven outside its negative common mode limit. When the 50pF unit's feedback decays, C1 again switches high and the entire cycle repeats. The oscillation frequency depends directly on the input-voltage-derived current.

Q1's emitter voltage must be carefully controlled to get low drift. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE}. The three LT1004s are the actual voltage reference and the LM334 current source provides 12µA bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by using the LM334's 0.3%/°C tempco to slightly temperature modulate the voltage drop in the Q2–Q4 trio. This correction's sign and magnitude directly oppose the –120ppm/°C 100pF polystyrene capacitor's drift,

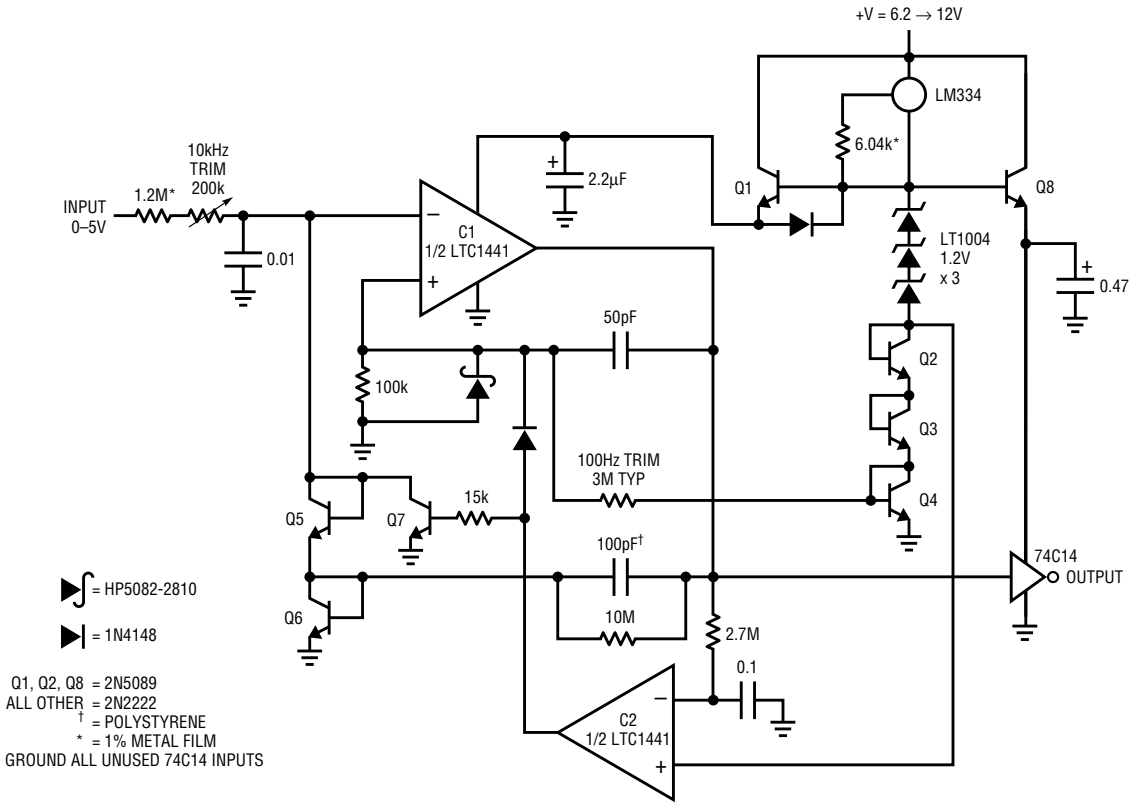


Figure 1. 0.02% V/F converter requires only 26µA supply current

aiding overall circuit stability. Q8's isolated 100pF drive to the CMOS inverter prevents output loading from influencing Q1's operating point. This makes circuit accuracy independent of loading.

The Q1 emitter-follower delivers charge to the 100pF capacitor efficiently. Both base and collector current end up in the capacitor. The 100pF capacitor, as small as accuracy permits, draws only small transient currents during its charge and discharge cycles. The 50pF–100k positive feedback combination draws insignificantly small switching currents. Figure 3, a plot of supply current versus operating frequency, reflects the low power design. At zero frequency, comparator quiescent current and the 12µA reference stack bias account for all current drain. There are no other paths for loss. As frequency scales up, the 100pF capacitor's charge-discharge cycle introduces the 1.1µA/kHz increase shown. A smaller value capacitor would cut power, but effects of stray capacitance and charge imbalance would introduce accuracy errors.

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes low; C2, detecting this via the 2.7M–0.1µF lag, goes high. This lifts C1's positive input and grounds the negative input with Q7, initiating normal circuit action.

To calibrate this circuit, apply 50mV and select the indicated resistor at C1's positive input for a 100Hz output. Complete the calibration by applying 5V and trimming the input potentiometer for a 10kHz output.

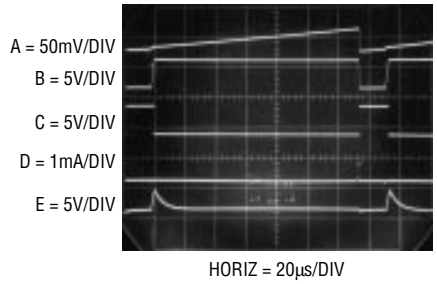


Figure 2. Waveforms for the micropower V/F converter: charge-based feedback provides precision operation with extremely low power consumption.

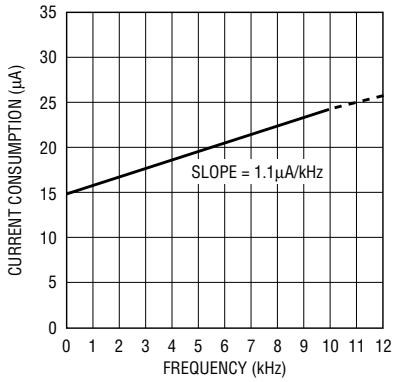


Figure 3. Current consumption versus frequency for the V/F converter: charge/discharge cycles account for 1.1µA/kHz current drain increase.

LT1210, continued from page 37

shutdown to cover the external transistors. The thermal shutdown of the LT1210 activates when the junction temperature reaches 150°C and has about 10°C hysteresis. The thermal resistance $R_{\theta JC}$ of the TO-220 package (LT1210CY) is 5°C/Watt).

Summary

The LT1210 is a great part; its performance in terms of speed, output current and output voltage is unsurpassed. Its C-Load™ output drive and thermal shutdown allow it to take its place in the real world—no kid gloves are required here. If the generous output specification of the LT1210 isn't big enough for your needs, just add a couple of transistors to dissipate the additional power and you are on your way. Only the worldwide supply of transistors limits the amount of power you could command with one of these parts.

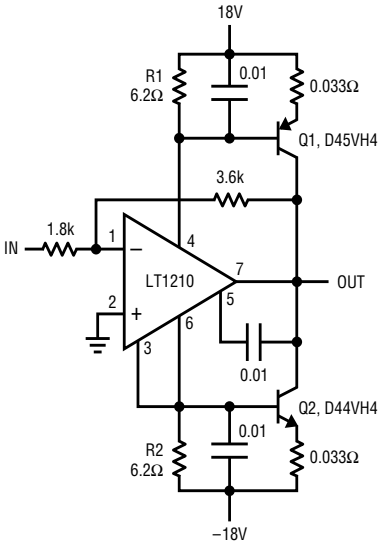


Figure 6. ±10A/1MHz current-boosted power op amp

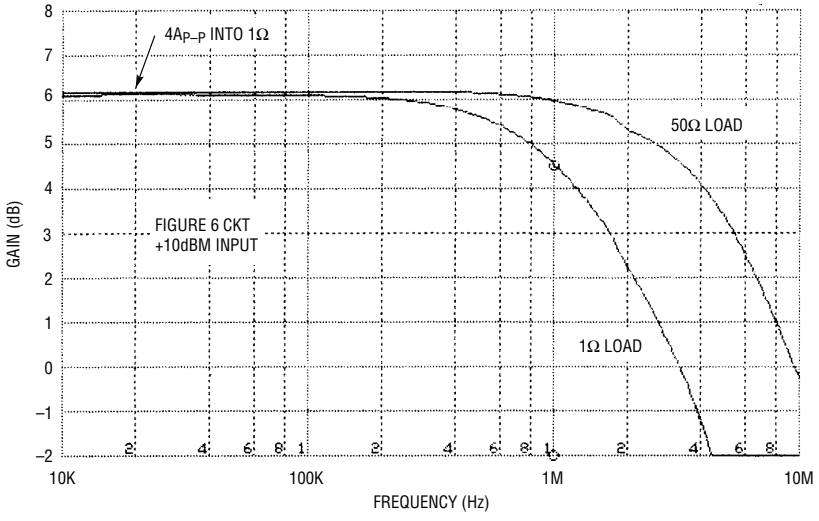


Figure 7. Gain versus frequency response of current-boosted amplifier

0.05µV/°C Chopped Amplifier Requires Only 5µA Supply Current

by Jim Williams

Figure 1 shows a chopped amplifier that requires only 5.5µA supply current. Offset Voltage is 5µV, with 0.05µV/°C drift. A gain exceeding 10^8 affords high accuracy, even at large closed-loop gains.

The micropower comparators (C1A and C1B) form a biphase 5Hz clock. The clock drives the input-related switches, causing an amplitude-modulated version of the DC input to appear at A1A's input. AC-coupled A1A takes a gain of 1000, presenting its output to a switched demodulator similar to the aforementioned modulator.

The demodulator output, a reconstructed, DC-amplified version of the circuit's input, is fed to A1B, a DC gain stage. A1B's output is fed back, via gain setting resistors, to the input modulator, closing a feedback loop around the entire amplifier. The configuration's DC gain is set by the feedback resistor's ratio, in this case 1000.

The circuit's internal AC coupling prevents A1's DC characteristics from influencing overall DC performance, accounting for the extremely low offset uncertainty noted. The high open-loop gain permits 10ppm gain accuracy at a closed-loop gain of 1000.

The desired micropower operation and A1's bandwidth dictate the 5Hz clock rate. As such, the resultant overall bandwidth is *low*. Full-power bandwidth is 0.05Hz with a slew rate of about 1V/s. Clock-related noise, about 5µV, can be reduced by increasing C_{COMP}, with commensurate bandwidth reduction.

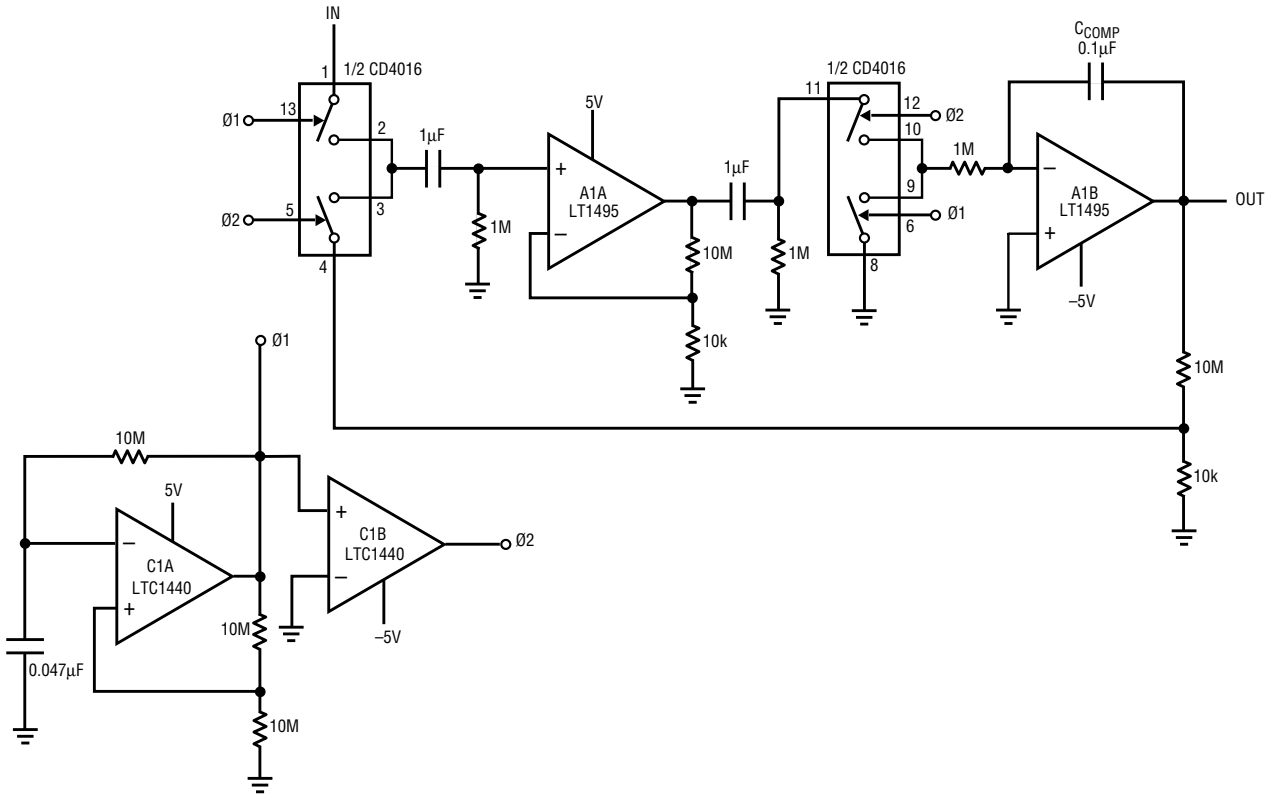


Figure 1. 0.05µV/°C chopped amplifier requires only 5µA supply current

LT1533 Ultralow Noise Switching Regulator for High Voltage or High Current Applications

by Jim Williams

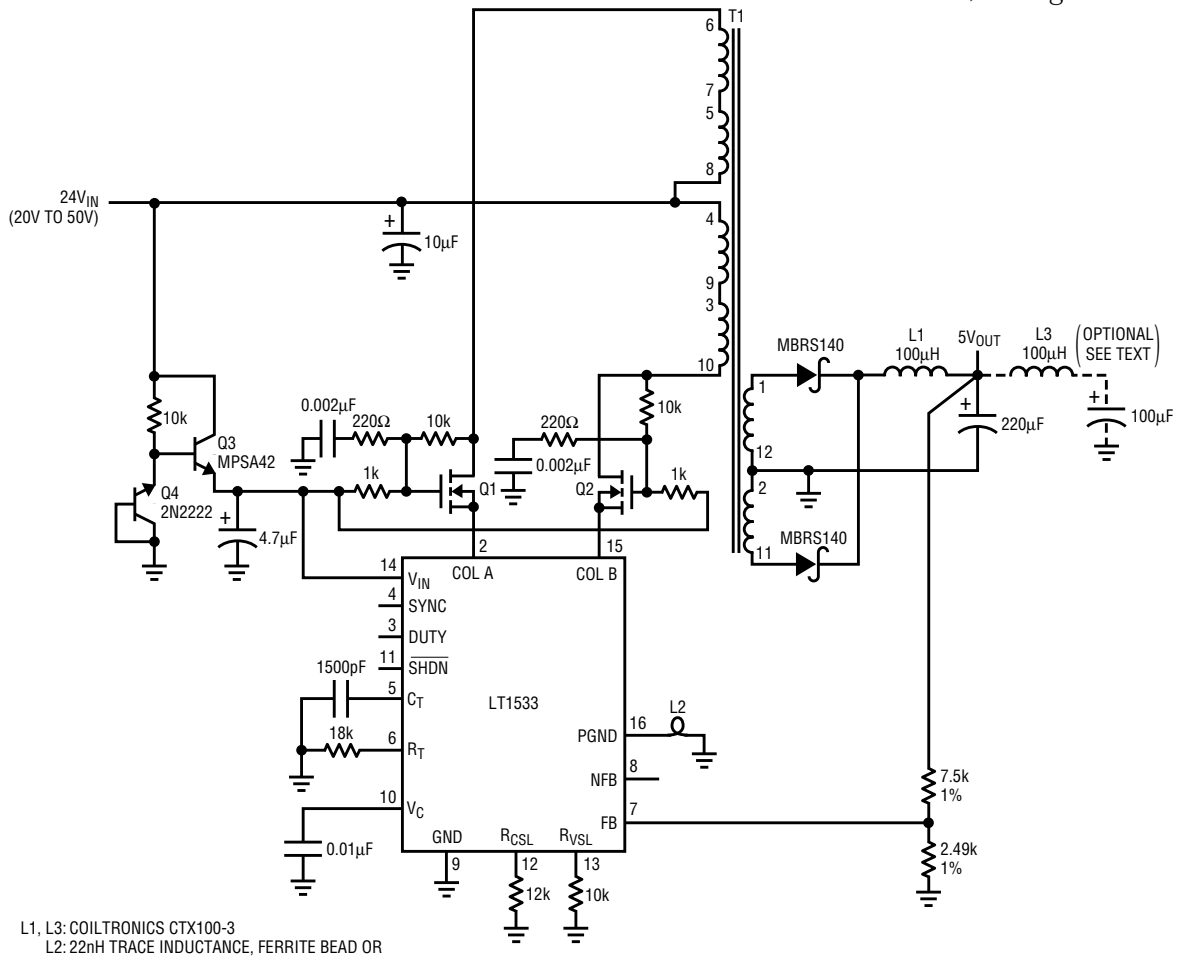
The LT1533 switching regulator[1, 2] achieves 100µV output noise by using closed-loop control around its output switches to tightly control switching transition time. Slowing down switch transitions eliminates high frequency harmonics, greatly reducing conducted and radiated noise.

The part's 30V, 1A output transistors limit available power. It is possible to exceed these limits while maintaining low noise performance by using suitably designed output stages.

High Voltage Input Regulator

The LT1533's IC process limits collector breakdown to 30V. A complicating factor is that the transformer causes the collectors to swing to twice the supply voltage. Thus, 15V represents the maximum allowable input supply. Many applications require higher voltage inputs; the circuit in Figure 1 uses a cascoded[3] output stage to achieve such high voltage capability. This 24V to 5V (V_{IN} = 20V–50V) converter is reminiscent of previous LT1533 circuits, except for the presence of Q1 and Q2.[4] These devices, interposed between the IC and the transformer, constitute a cascoded high voltage stage. They provide voltage gain while isolating the IC from their large drain voltage swings.

Normally, high voltage cascodes are designed to simply supply voltage isolation. Cascoding the LT1533 presents special considerations because the transformer's instantaneous voltage and current information must be accurately transmitted, albeit at lower amplitude, to the LT1533. If this is not done, the regulator's slew-control



L1, L3: COILTRONICS CTX100-3
L2: 22nH TRACE INDUCTANCE, FERRITE BEAD OR INDUCTOR COILCRAFT B-07T TYPICAL
Q1, Q2: MTD6N15
T1: COILTRONICS VP4-0860

Figure 1. A low noise 24V to 5V converter (V_{IN} = 20V–50V): cascoded MOSFETs withstand 100V transformer swings, permitting the LT1533 to control 5V/2A output.

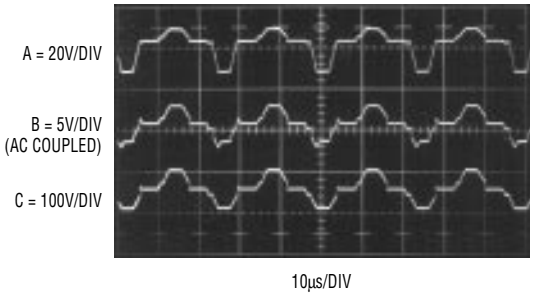


Figure 2. MOSFET-based cascode permits the regulator to control 100V transformer swings while maintaining a low noise 5V output. Trace A is Q1's source, Trace B is Q1's gate and Trace C is the drain. Waveform fidelity through cascode permits proper slew-control operation.

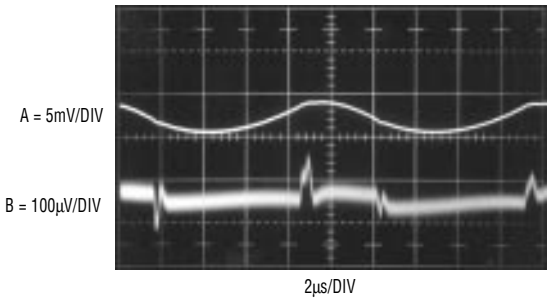


Figure 4. Waveforms for Figure 3 at 10W output: Trace A shows fundamental ripple with higher frequency residue just discernible. The optional LC section results in Trace B's 180µV_{P-P} wideband noise performance.

loops will not function, causing a dramatic output noise increase. The AC-compensated resistor dividers associated with the Q1–Q2 gate-drain biasing serve this purpose, preventing transformer swings coupled via gate-channel capacitance from corrupting the cascode's waveform-transfer fidelity. Q3 and associated components provide a stable DC termination for the dividers while protecting the LT1533 from the high voltage input.

Figure 2 shows that the resultant cascode response is faithful, even with 100V swings. Trace A is Q1's source; traces B and C are its gate and drain, respectively. Under these conditions, at 2A output, noise is inside 400µV peak.

Current Boosting

Figure 3 boosts the regulator's 1A output capability to over 5A. It does this with simple emitter followers (Q1–Q2). Theoretically, the followers preserve T1's voltage and current waveform information, permitting the LT1533's slew-control circuitry to function. In practice, the transistors must be relatively low beta types. At 3A collector current, their beta of 20 sources ≈150mA via the Q1–Q2 base paths, adequate for proper slew-loop operation.[5] The follower loss limits efficiency to about 68%. Higher input voltages minimize follower-induced loss, permitting efficiencies in the low 70% range.

Figure 4 shows noise performance. Ripple measures 4mV (Trace A) using a single LC section, with high frequency content just discernible. Adding the optional second LC section reduces ripple to below 100µV (trace B), and high frequency content is seen to be inside 180µV (note ×50 vertical scale-factor change).

Notes:

1 Witt, Jeff. The LT1533 Heralds a New Class of Low Noise Switching Regulators. *Linear Technology* VII:3 (August 1997).

2 Williams, Jim. *LTC Application Note 70: A Monolithic Switching Regulator with 100µV Output Noise*. October 1997.

3 The term "cascode," derived from "cascade to cathode," is applied to a configuration that places active devices in series. The benefit may be higher breakdown voltage, decreased input capacitance, bandwidth improvement or the like. Cascoding has been employed in op amps, power supplies, oscilloscopes and other areas to obtain performance enhancement.

4 This circuit derives from a design by Jeff Witt of Linear Technology Corp.

5 Operating the slew loops from follower base current was suggested by Bob Dobkin of Linear Technology Corp.

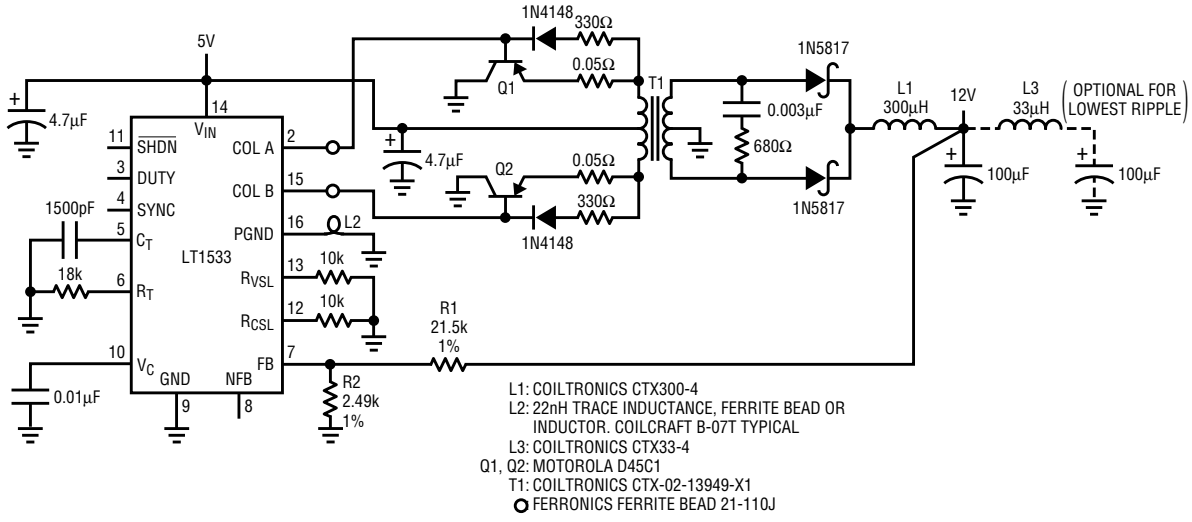


Figure 3. A 10W low noise 5V to 12V converter: Q1–Q2 provide 5A output capacity while preserving the LT1533's voltage/current slew control. Efficiency is 68%. Higher input voltages minimize follower loss, boosting efficiency above 71%.

A 7ns, 6mA, Single-Supply Comparator Fabricated on Linear's 6GHz Complementary Bipolar Process

by Jim Williams and Brian Hamilton

Introduction

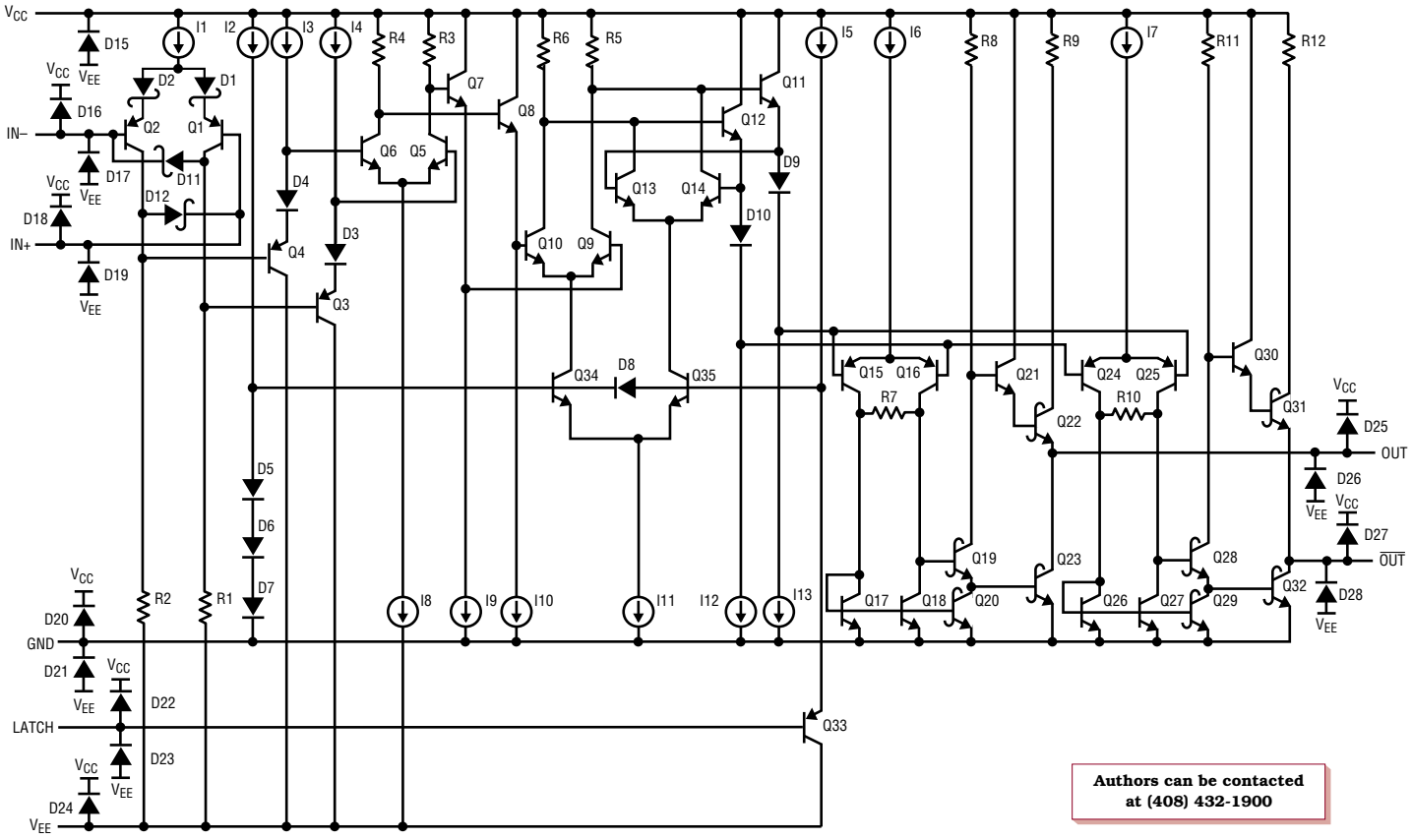
The LT1394 is an ultrafast (7ns), low power (6mA), single-supply comparator designed to operate on either 5V or ±5V supplies. It has a maximum offset voltage of 2.5mV, complementary TTL compatible outputs and output latch capability. The LT1394 is the first product made with Linear Technology's 6GHz complementary bipolar technology. This fine-line geometry process results in a product with dramatically improved speed and power compared to industry-standard comparators developed in slower NPN-only technologies.

These features combine to make the LT1394 well suited for applications such as high performance NTSC crystal oscillators, single-supply voltage-to-frequency converters and high speed, high accuracy level detectors. The LT1394 is offered in SO-8 and is pin compatible with the industry-standard LT1016 and LT1116 comparators.

Circuit Description

A simplified schematic of the LT1394 can be seen in Figure 1. There are differential inputs (+IN/–IN), differential outputs (OUT/$\overline{OUT}$), a latch input (LATCH) and three power supply pins (V_{EE}, V_{CC} and GND). The circuit topology consists of a differential input stage, a level-shifting gain stage, a latch stage and complementary output stages. The complementary output stages offer improved flexibility for the user; the latch stage provides superior sampling accuracy of the input signal without the need for an external latch.

The input stage of the LT1394 uses a PNP differential pair (Q1–Q2) with Schottky diodes in the emitters (D1–D2) and resistive loads (R1–R2). The Schottky diodes in series with the emitters allow differential input voltages that are greater than the base-emitter breakdown of the input transistors. Two additional Schottky



Authors can be contacted at (408) 432-1900

Figure 1. LT1394 simplified schematic

diodes (D11–D12) prevent output phase reversal when either input is taken far enough below V_{EE} to forward bias the base-collector junction of its corresponding PNP input transistor. To allow single-supply operation, the input stage has been designed to have small voltage swings across load resistors R1 and R2. This ensures that the input PNPs will not saturate with the LT1394 inputs at V_{EE}.

The signal path remains differential as it is buffered and level shifted via transistors Q3–Q4 and diodes D3–D4. The level shift prevents current source I_8 from saturating. The second gain stage, comprising transistors Q5–Q6 and resistors R3–R4, takes additional gain while level shifting the signal back to V_{CC}. The differential output of the second gain stage is buffered by transistors Q7–Q8, which then drive the latch stage.

In the latch stage, transistors Q9–Q10 and resistors R5–R6 act as a third gain stage. Q11–Q12 buffer the signal at resistors R5–R6, driving another differential pair (Q13–Q14). Q13 and Q14, when activated, provide positive feedback to resistors R5–R6, creating the latch. When the LATCH pin is low, the LT1394 is in flow-through or GAIN mode. Current I_{11} is steered through Q34, activating the Q9–Q10 differential pair. When the LATCH pin is high, the LT1394 is in LATCH mode. Current I_{11} is steered through Q35, activating the Q13–Q14 differential pair. The output of the gain/latch stage has additional level shifting from the emitters of transistors Q11–Q12 via diodes D9–D10. This level shifting prevents the output stage current sources I_6 and I_7 from saturating.

The LT1394 provides complementary outputs by using two identical output stages connected in opposite phases. Examining the output circuitry for the OUT pin, a PNP differential pair (Q15–Q16) is driven from the outputs of the latch stage. When I_6's current is steered through Q16, it drives R7 and the base of Q19. R7 improves switching speed by reducing the gain of the differential pair Q15–Q16 and lowering the impedance at the base of Q19. Q19's emitter current then drives the base of Q23, turning it on until the OUT pin has been pulled low and Q23's Schottky clamp diode has turned on. Conversely, if I_6's current is steered through Q15, it allows R8 to pull up the Darlington-connected output transistors Q21 and Q22, bringing the OUT pin high. For faster output switching times, Q15's collector current flows into the Q17/Q18/Q20 current mirror. Q20's collector current helps turn off Q23, whereas the collector current of Q18 helps turn off Q19.

Linear Technology's 6GHz Complementary Bipolar Technology

Linear Technology's 6GHz complementary bipolar technology (6GHz ComBi) features vertical NPN and PNP transistors with similar frequency response and gain characteristics. Both the NPN and PNP transistors feature polysilicon emitters for improved gain, a collector-to-emitter breakdown voltage (BV_{CEO}) greater than 12V and a unity gain frequency (f_T) of 6GHz. The PNP transistors have a nominal current gain (β) of about 45, while the NPNs have a β of about 100.

In addition to the transistors, the 6GHz ComBi technology includes diode, resistor and capacitor structures. Schottky barrier diodes with low parasitic capacitance and high breakdown voltage are included for high speed voltage clamping and breakdown protection of transistors. Low parasitic capacitance polysilicon resistors are included for use in high speed signal paths. High resistivity diffused resistors are used for biasing and low power circuitry. Polysilicon-oxide-metal capacitors offer low parasitic capacitance, high capacitance density and low series resistance for good high frequency performance.

When compared to a typical 30V complementary bipolar process, the reduction of transistor BV_{CEO} from 30V to 12V has many benefits for applications that do not require higher supply voltages. Dramatically reduced depletion widths within the transistor allow a 50% decrease in area. This area reduction improves speed by lowering parasitic capacitances associated with the transistor. The reduced voltage requirement also allows a thinner, richer epitaxial (epi) region. This change to the epi region dramatically reduces the collector resistance of the transistors, resulting in smaller

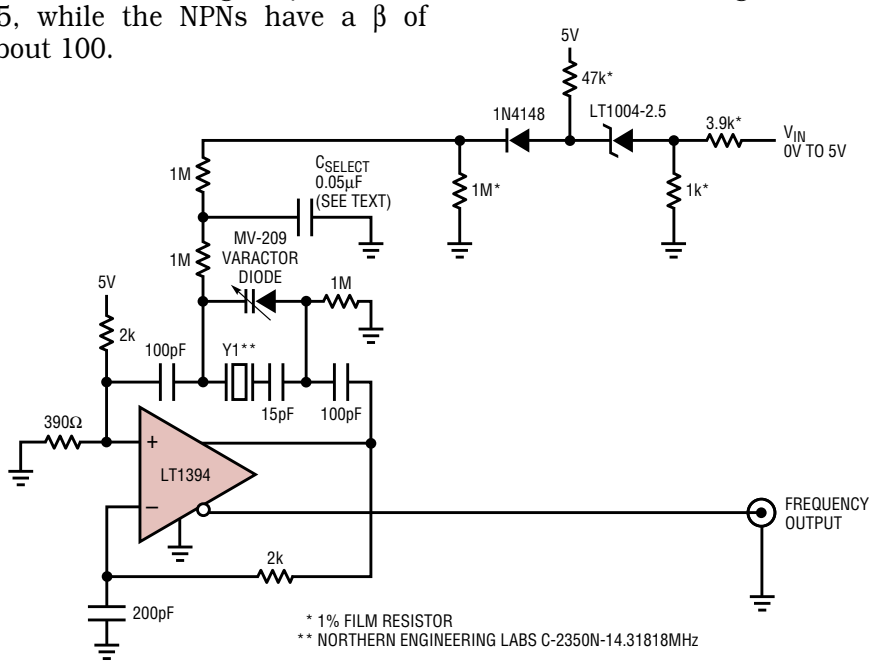


Figure 2. A 4× NTSC subcarrier voltage tunable crystal oscillator; tuning range and bandwidth accommodate a variety of phase-locked loops.

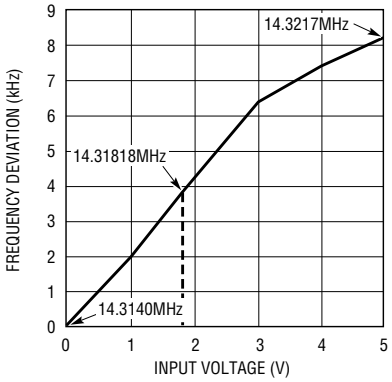


Figure 3. Control voltage vs output frequency for Figure 2; tuning deviation from the center frequency exceeds ±240ppm.

transistors for a given current level. With this significant reduction in transistor size, interconnects using a single metallization layer becomes much more difficult and would generate significant parasitic capacitance. Because of this, the 6GHz ComBi process utilizes two levels of metallization.

Applications

4× NTSC Voltage-Tunable Crystal Oscillator

The first of three representative applications for the LT1394 can be seen in Figure 2. This circuit is a crystal oscillator with voltage tuning of the output frequency. This application makes use of the LT1394's high speed, complementary outputs and single-supply 5V operation. Such voltage controlled crystal oscillators (VCXO) are often employed where slight variation of a stable carrier is required. This example is specifically intended to provide a 4× NTSC subcarrier tunable oscillator suitable for phase locking.

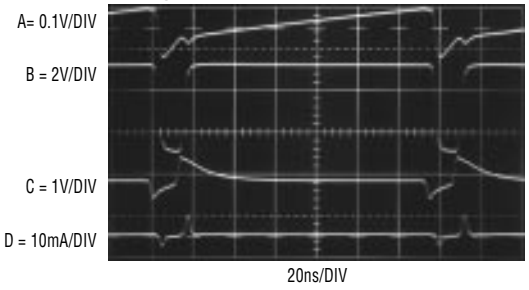


Figure 5. Waveforms for the 10MHz voltage-to-frequency converter; charge pump–based feedback provides linearity and fast response to input.

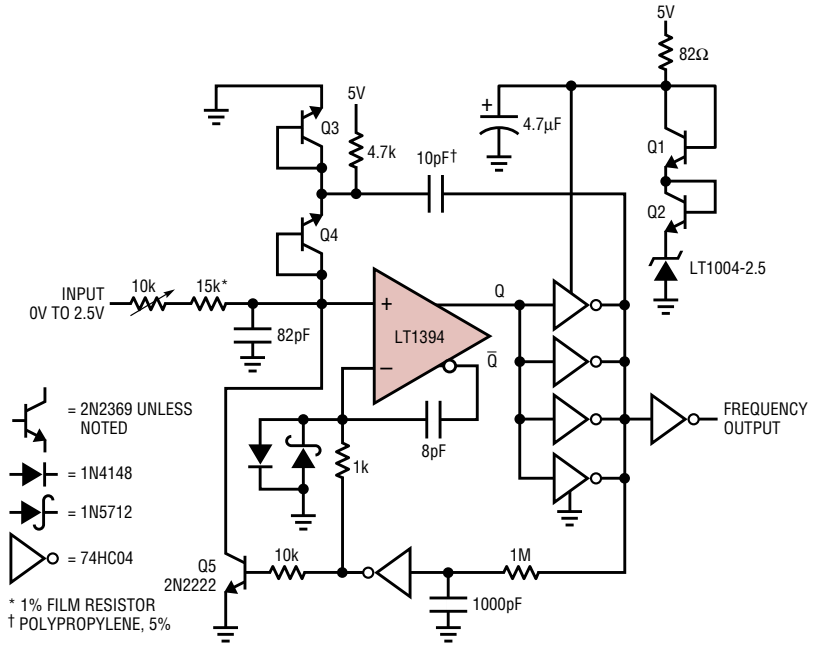


Figure 4. This simple charge pump–based 10MHz voltage-to-frequency converter has 40dB dynamic range and operates from a 5V supply.

The resistors at the LT1394's positive input set a DC bias point of 840mV. The 2kΩ– 200pF path sets up phase-shifted negative feedback, putting the DC output in the active region with a gain of 35 at the oscillation frequency. The crystal's path provides resonant positive feedback and stable oscillation occurs. The varactor diode is biased from the tuning input. The tuning network is arranged so that a 0V to 5V drive provides a reasonably symmetric, broad tuning range around the 14.31818MHz center frequency. The capacitor labeled C_{SELECT} sets the tuning bandwidth. It should be picked to complement loop response in phase-locking applications. Figure 3 is a plot of frequency deviation versus tuning input voltage. Tuning deviation from the 4× NTSC 14.31818MHz center frequency ex-

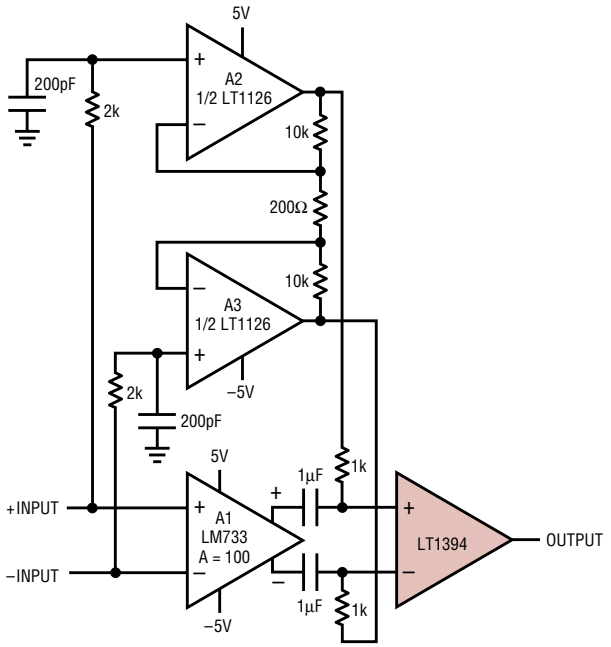


Figure 6. Parallel preamplified paths allow 18ns response to 500µV overdrive.

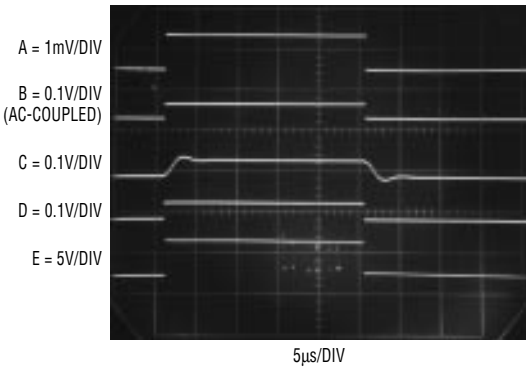


Figure 7. 500µV input (Trace A) is split into wideband and low frequency gain paths (Traces B and C) and recombined (Trace D). Trace E is the level-detector output.

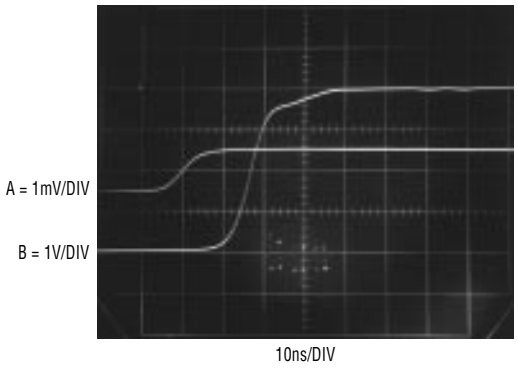


Figure 8. Parallel-path level detector shows 18ns response (Trace B) to 500µV overdrive (Trace A).

ceeds ±240ppm for a 0V to 5V tuning range.

Simple 10MHz Single-Supply V/F Converter

A second application for the LT1394 is shown in Figure 4. It is a simple 10MHz single-supply voltage-to-frequency converter that makes use of the LT1394's speed, single-supply operation and complementary outputs. A 0V to 2.5V input produces a 0Hz to 10MHz output with 40dB of dynamic range, 1% linearity and 400 ppm/°C gain drift. Power supply rejection is 0.5% for 4.75V to 5.25V supply excursions.

To understand circuit operation, assume the LT1394's positive input is slightly below its negative input. The circuit's input voltage causes a positive-going ramp at the comparator's positive input (Trace A, Figure 5). The Q output is low, forcing the CMOS inverter outputs high. This allows current flow from diode Q1's collector, through the CMOS inverter supply pin, to the 10pF capacitor. The 4.7µF capacitor provides high frequency bypass, maintaining low impedance at Q1's collector. Diode connected Q3 provides a path to ground. The voltage to which the 10pF capacitor charges is a function of Q1's collector potential and Q3's drop. When the ramp at the comparator's positive input goes high enough, the Q output goes high and the paralleled inverters switch low (Trace B). This action pulls current from the 82pF capacitor at the input via the Q1–10pF route (Trace D). This current removal resets the LT1394's positive input ramp to a potential slightly below ground, forcing the Q output low and the paralleled inverters high. The 8pF capacitor at the LT1394's inverting output furnishes AC positive feedback to the negative input (Trace C). This ensures that the Q output remains high long enough for a complete discharge of the 10pF capacitor. The Schottky diode prevents the LT1394's input from being driven outside its negative common mode limit. When the 8pF capacitor's feedback decays, the LT1394 again switches and the entire cycle repeats. The oscillation frequency depends entirely upon the input-derived current. The LT1004 is the circuit's voltage reference, with Q1 and Q2 temperature compensating Q3 and Q4.

Start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, the LT1394's output goes high, causing the paralleled inverters to go low. After a time determined by the 1MΩ–1000pF RC, the associated lone inverter goes high. This lifts the LT1394's negative input and grounds the positive input with Q5, initiating normal circuit action.

To calibrate this circuit, apply 2.5V and adjust the 10k potentiometer for a 10MHz output.

18ns 500µV Level Detector

The ultimate limitation on comparator sensitivity is available gain. Unfortunately, increasing gain invariably involves giving up speed. The gain vs speed trade-off in fast comparators is usually a practical compromise designed to satisfy most applications. Some situations, however, require more sensitivity (that is, higher gain) with minimal effect on speed. Figure 6's circuit adds a differential preamplifier ahead of the LT1394, increasing gain. This permits 500µV comparisons in 18ns. A parallel-path DC stabilization approach eliminates preamplifier drift as an error source. A1 is the differential amplifier, operating at a gain of 100. Its output is AC coupled to the LT1394. A1 has poorly defined DC characteristics, necessitating some form of DC correction. A2 and A3, operating at a differential gain of 100, provide this function. They differentially sense a band-limited version of A1's inputs and feed DC and low frequency amplified information to the comparator. The low frequency roll-off of A1's signal path complements A2–A3's high frequency roll-off. The summation of these two signal channels at the LT1394's inputs results in flat response from DC to high frequency.

Figure 7 shows waveforms for the high sensitivity level detector. Trace A is a 500µV overdrive on a 1mV step applied to the circuit's positive input (negative input grounded). Trace B shows the resulting amplified step at A1's positive output. Trace C is A2's

band-limited output. A1's wideband output combines with A2's DC-corrected information to yield the correct, amplified composite signal at the LT1394's positive input in Trace D. The LT1394's output is Trace E. Figure 8 details circuit propagation delay. The output responds in 18ns to a 500µV overdrive on a 1mV step. Figure 9 plots response time versus overdrive. As might be expected, propagation delay decreases at higher overdrives. A1's noise limits usable sensitivity.

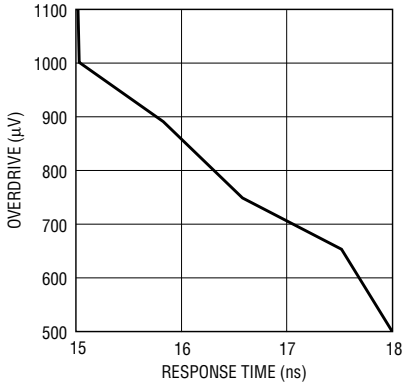


Figure 9. Response time vs overdrive for the composite level detector

Conclusion

Innovative circuit design, coupled with Linear Technology's 6GHz complementary bipolar process simultaneously achieves the seemingly contradictory goals of high speed and low power. The LT1394 is easy to use, thanks to its single-supply capability and complementary outputs. Additional LT1394 applications appear in the forthcoming Linear Technology Application Note, *A Seven Nanosecond Comparator for Single Supply Operation.*

LTC1401/LTC1404, continued from page 19

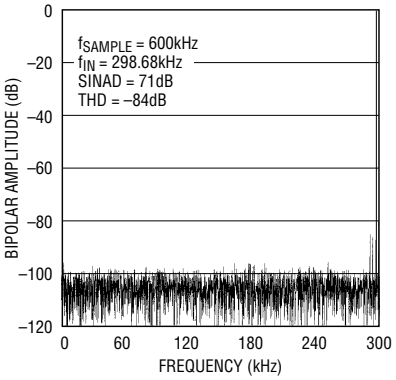


Figure 6a. LTC1404 FFT

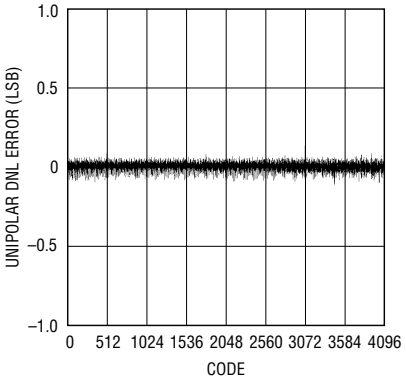


Figure 6b. LTC1404 DNL error

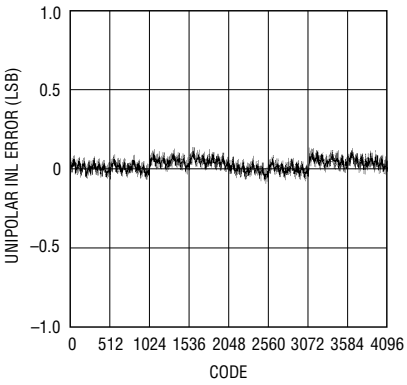


Figure 6c. LTC1404 INL error

Applications

The LTC1401 and LTC1404 will find applications in telecommunications, digital signal processing, portable-computer data acquisition boards and high speed or multiplexed data acquisition.

In telecommunication applications such as HDSL (high-bit-rate digital subscriber line interface), high speed and low power dissipation are a must because the systems are usually powered by the phone line itself. Excellent dynamic performance is required of the ADC's sample-and-hold. The serial interface minimizes the number of signal lines that must be routed, thereby saving significant board space. The 600ksps LTC1404, with its SO-8 footprint, is an excellent choice for HDSL applications. At 584ksps, with 2B1Q coding, the LTC1404 receives at 2.048Mbps over two wires.

Another common use of ADCs is in data acquisition applications. System designers have always faced problems in optimizing data acquisition applications for speed, size, power and cost, especially in the case of portable designs. The high sample rate, the high level of functional integration and the low cost of these converters make them ideal choices for these applications. The LTC1401 and LTC1404 can be easily interfaced to a low cost MUX (for example, a CD4051, 74HC4051 or LTC1391) through their high impedance inputs. The high input impedance of these ADCs eliminates the need for a buffer between the MUX and the ADC, resulting in savings of both cost and board space.

Conclusion

The new LTC1401 and LTC1404 come with full ADC performance and an easy-to-use serial interface. These complete, stand alone, high speed, low power devices will simplify the job of system designers.

Component and Measurement Advances Ensure 16-Bit DAC Settling Time (Part One)

by Jim Williams

Introduction

Instrumentation, waveform generation, data acquisition, feedback control systems and other application areas are beginning to utilize 16-bit data converters. More specifically, 16-bit digital-to-analog converters (DACs) have seen increasing use. New components (see the sidebar "Components for 16-Bit Digital-to-Analog Conversion" on page 31) have made 16-bit DACs a practical design alternative. These ICs provide 16-bit performance at reasonable cost compared to previous modular and hybrid technologies. The DC and AC specifications of the monolithic DACs approach or equal previous converters at significantly lower cost.

DAC Settling Time

DAC DC specifications are relatively easy to verify. Measurement techniques are well understood, albeit often tedious. AC specifications require more sophisticated approaches to produce reliable information. In particular, the settling time of the DAC and its output amplifier is extraordinarily difficult to determine to 16-bit resolution. DAC settling time is the elapsed time from input code application until the output arrives at and remains within a specified error band around the final value. It is usually specified for a full-scale 10V transition. Figure 1 shows that DAC settling time has three distinct components. The *delay time* is very small and is almost entirely due to propagation delay through the DAC and output amplifier. During this interval there is no output movement. During *slew time* the output amplifier moves at its highest possible speed towards the final value. *Ring time* defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. There is normally a trade-off between slew and ring time. Fast-slewing amplifiers generally have extended ring times, complicating amplifier choice and frequency compensation. Additionally, the architecture of very fast amplifiers usually dictates trade-offs that degrade DC error terms.

Measuring anything at any speed to 16 bits (≈0.0015%) is hard. Dynamic measurement to 16-bit resolution is particularly challenging. Reliable 16-bit settling-time measurement constitutes a high order difficulty problem requiring exceptional care in approach and experimental technique.

Considerations for Measuring DAC Settling Time

Historically, DAC settling time has been measured with circuits similar to that in Figure 2. The circuit uses the "false sum node" technique. The resistors and DAC-amplifier form a bridge-type network. Assuming ideal resistors, the amplifier output will step to V_{IN} when the DAC inputs move to all ones. During slew, the settle node is bounded by the diodes, limiting voltage excursion. When settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half of the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. The oscilloscope connection presents problems. As probe capacitance rises, AC loading of the resistor junction influences observed settling waveforms. A 10pF probe alleviates this problem but its 10× attenuation sacrifices oscilloscope gain. 1× probes are not suitable because of their excessive input capacitance. An active

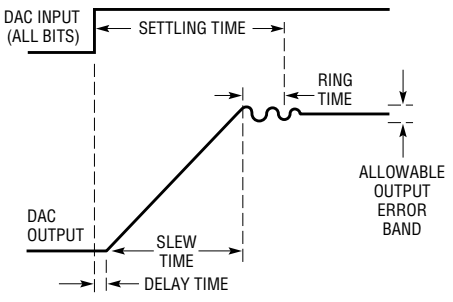


Figure 1. DAC-settling-time components include delay, slew and ring times. Fast amplifiers reduce slew time, although longer ring time usually results. Delay time is normally a small term.

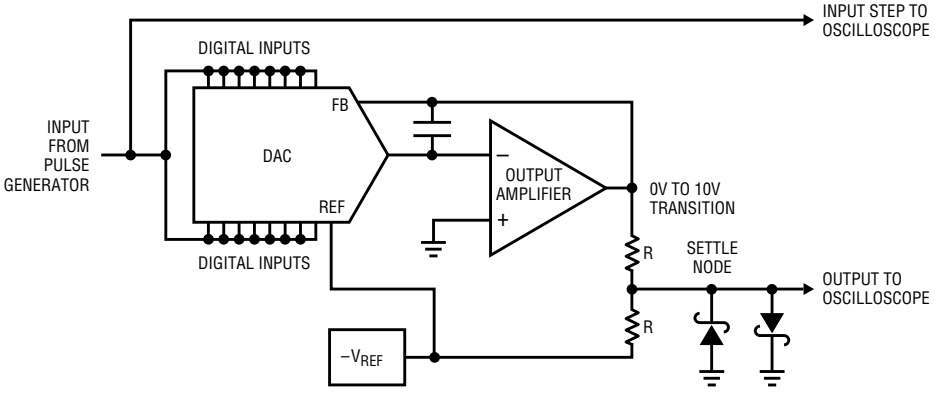


Figure 2. Popular summing scheme for DAC-settling-time measurement provides misleading results. 16-bit measurement causes >200× oscilloscope overdrive. Displayed information is meaningless.

Components for 16-Bit D/A Conversion

Components suitable for 16-bit D/A conversion are members of an elite class. 16 binary bits is one part in 65,536—just 0.0015% or 15 parts-per-million. This mandates a vanishingly small error budget and the demands on components are high. The digital-to-analog converters listed in Table A all use Si-Chrome thin-film resistors for high stability and linearity over temperature. Gain drift is typically 1ppm/°C or about 2LSBs over 0°C to 70°C. The amplifiers shown contribute less than 1LSB error over 0°C to 70°C with 16-bit DAC driven settling times of 1.7µs available. The references offer drifts as low as 1LSB over 0°C to 70°C with initial trimmed accuracy to 0.05%

Table A. Short-form descriptions of components suitable for 16-bit digital-to-analog conversion

Component Type	Error Contribution Over 0°C to 70°C	Comments
LTC1597 DAC	≈2LSB Gain Drift 1LSB Linearity	Full Parallel Inputs Current Outputs
LTC1595 DAC	≈2LSB Gain Drift 1LSB Linearity	Serial Input 8-Pin Package Current Output
LTC1650 DAC	≈3.5LSB Gain Drift 6LSB Offset 4LSB Linearity	Complete Voltage Output DAC
LT1001 Amplifier	<1LSB	Good Low Speed Choice 10mA Output Capability
LT1012 Amplifier	<1LSB	Good Low Speed Choice Low Power Consumption
LT1468 Amplifier	<2LSB	1.7µs Settling to 16 Bits Fastest Available
LM199A Reference: 6.95V	≈1LSB	Lowest Drift Reference in this Group
LT1021 Reference: 10V	≈4LSB	Good General Purpose Choice
LT1027 Reference: 5V	≈4LSB	Good General Purpose Choice
LT1236 Reference: 10V	≈10LSB	Trimmed to 0.05% Absolute Accuracy
LT1461 Reference: 4.096V	≈10LSB	Recommended for LTC1650 DACs (see Above)

1× FET probe will work, but another issue remains.

The clamp diodes at the settle node are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The Schottky diodes' 400mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question.

At 10-bit resolution (10mV at the DAC output—5mV at the oscilloscope), the oscilloscope typically undergoes a 2× overdrive at 50mV/DIV and the desired 5mV baseline is just discernible. At 12-bit or higher resolution, the measurement becomes hopeless with this arrangement. Increasing oscilloscope gain brings commensurate increased vulnerability to overdrive induced errors. At 16 bits, there is clearly no chance of measurement integrity.

The preceding discussion indicates that measuring 16-bit settling time requires a high gain oscilloscope that is somehow immune to overdrive. The gain issue is addressable with an external wideband preamplifier that accurately amplifies the diode-clamped settle node. Getting around the overdrive problem is more difficult.

The only oscilloscope technology that offers inherent overdrive immunity is the classical sampling 'scope.

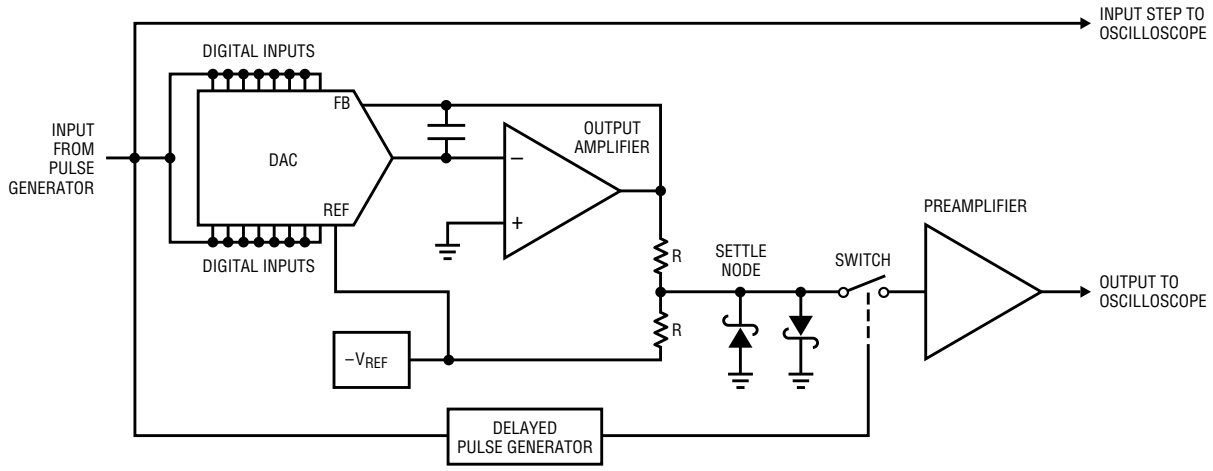


Figure 3. Conceptual arrangement eliminates oscilloscope overdrive. A delayed pulse generator controls the switch, preventing the oscilloscope from monitoring settle node until settling is nearly complete.

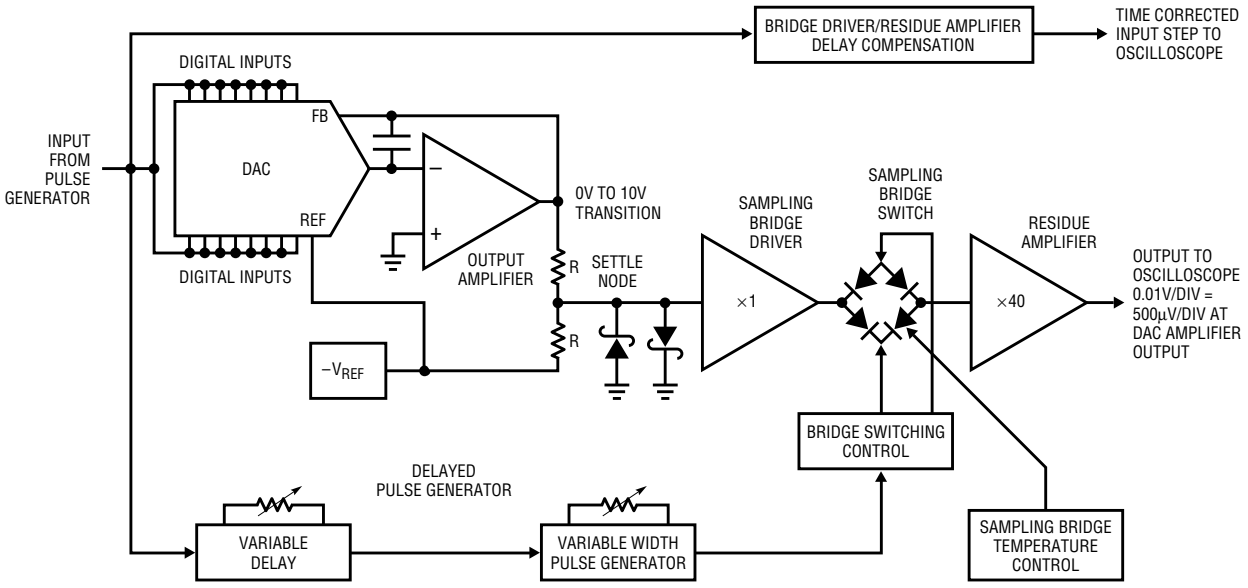


Figure 4. Block diagram of DAC-settling-time measurement scheme: diode bridge switch minimizes switching feedthrough, preventing residue-amplifier oscilloscope overdrive. Temperature control maintains 10µV switch offset baseline. Input step-time reference is compensated for ×1 and ×40 amplifier delays.

Unfortunately, these instruments are no longer manufactured (although still available on the secondary market). It is possible, however, to construct a circuit that borrows the overload advantages of classical sampling 'scope technology. Additionally, the circuit can be endowed with features particularly suited for measuring 16-bit DAC settling time.

Practical DAC-Settling-Time Measurement

Figure 3 is a conceptual diagram of a 16-bit DAC-settling-time measurement circuit. This figure shares attributes with Figure 2, although some new features appear. In this case, the preamplified oscilloscope is connected to the settle point by a switch. The switch state is determined by a delayed pulse generator, which is triggered from the same pulse that controls the DAC. The delayed pulse generator's timing is arranged so that the switch does not close until settling is very nearly complete. In this way the incoming waveform is sampled in time, as well as amplitude. The oscilloscope is never subjected to overdrive—no off-screen activity ever occurs.

Figure 4 is a more complete representation of the DAC settling time scheme. Figure 3's blocks appear in greater detail and some new refinements show up. The DAC-amplifier summing area is unchanged. Figure 3's delayed pulse generator has been split into two blocks; a delay and a pulse generator, both independently variable. The input step to the oscilloscope runs through a section that compensates for the propagation delay of the settling-time-measurement path. The most striking new aspect of the diagram is the diode bridge switch. Borrowed from classical sampling oscilloscope circuitry, it is the key to the measurement. The diode bridge's inherent balance eliminates charge-injection-based errors in the output. It is far superior to other electronic switches in this characteristic. Any other high speed switch technology contributes excessive output spikes due to charge-based feedthrough. FET switches are not suitable because their gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt the oscilloscope display, inducing overload and defeating the switch's purpose.

The diode bridge's balance, combined with matched, low capacitance, monolithic diodes and complementary high speed switching, yields a cleanly

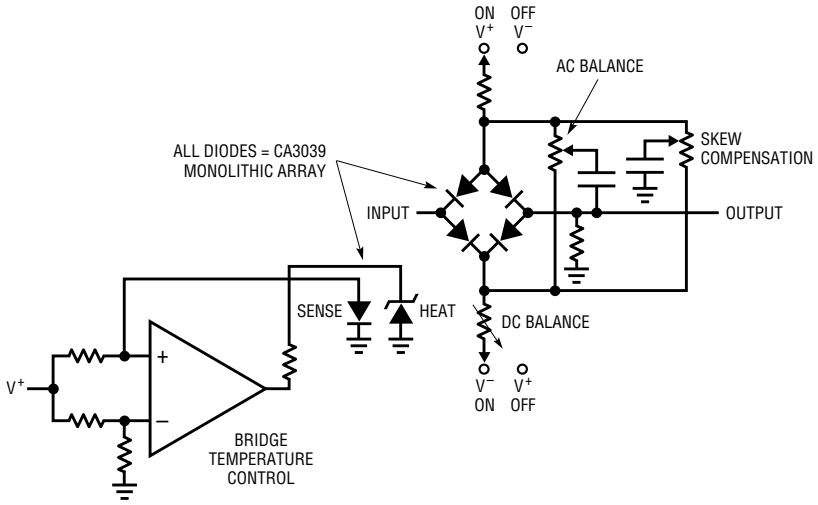


Figure 5. Diode bridge switch trims include AC and DC balance and switch drive timing skew. Remaining diodes in monolithic array are used for temperature control.

switched output. The monolithic diode bridge is also temperature controlled, providing a bridge offset error below 10µV, stabilizing the measurement baseline. The temperature control is implemented using uncommitted diodes in the monolithic array as heater and sensor.

Figure 5 details considerations for the diode bridge switch. The bridge diodes tend to cancel each other's temperature coefficient—unstabilized bridge drift is about 100µV/°C and the temperature control reduces residual drift to a few microvolts/°C.

Bridge temperature control is achieved by using one diode as a sensor. Another diode, running in reverse breakdown ($V_Z \approx 7V$), serves as the heater. The control amplifier, comparing the sensor diode to a voltage at its negative terminal, drives the heater diode to temperature stabilize the array.

DC balance is achieved by trimming the bridge on-current for zero input–output offset voltage. Two AC trims are required. The "AC balance" corrects for diode and layout capacitive imbalances and the "skew compensation" corrects for any timing asymmetry in the nominally complementary bridge drive. These AC trims compensate small dynamic imbalances that could result in parasitic bridge outputs.

Conclusion

This concludes part one of this article. Part two, which will appear in the November issue of *Linear Technology* magazine, details the settling time circuitry and presents results. Both parts represent a distillation of a full-length LTC application note, *AN74, Component and Measurement Advances Ensure 16-Bit DAC Settling Time.*

New 16-Bit Bipolar Output DAC in Narrow SO-16 Package

by Hassan Malik

Linear Technology introduces its first bipolar, voltage output 16-bit digital to analog converter, the LTC1650. The LTC1650 is available in a narrow 16-pin SO package, making it the smallest bipolar, 16-bit voltage output DAC on the market today. The LTC1650 operates from ± 5V supplies and draws 5mA. It is equipped with a rail-to-rail, low noise, deglitched output amplifier that can be configured to operate in a unipolar or bipolar mode. The mid-scale glitch is under 2nV-s and the full-scale settling time in unipolar mode is 4µs.

The LTC1650 is 16-bit monotonic over the industrial temperature range, with a typical differential nonlinearity of less than ±0.3LSB. Figures 1 and 2 show a typical application for the part and its DNL curve. The LTC1650 is equipped with an output-span-setting resistor tied to the UNI/BIP pin. When this pin is tied to the V_{OUT} pin, the output will swing from REFLO to REFHI; when the pin is tied to REFHI, the output swings from –REFHI to REFHI.

The LTC1650 has a user-defined voltage to which its output resets on power-up or when the part is cleared. The voltage on the V_{RST} pin is applied to the output through a transmission gate when the part powers up or is cleared. There are supply brown-out detectors on all three supplies, AV_{DD}, DV_{DD} and AV_{SS}. When any of these supplies drops below 2.5V, the part is cleared, connecting the output to V_{RST}, and the $\overline{RSTOUT}$ pin changes to a logic low.

The 3-wire serial interface of the LTC1650 is SPI/QSPI and MICROWIRE™ compatible. All the logic inputs are TTL/CMOS compatible and the CLK input is equipped with a Schmitt trigger that allows direct optocoupler interfacing. There is also a D_{OUT} pin for daisy-chaining several DACs. The digital feedthrough is 0.05nV-s.

MICROWIRE is a trademark of National Semiconductor Corp.

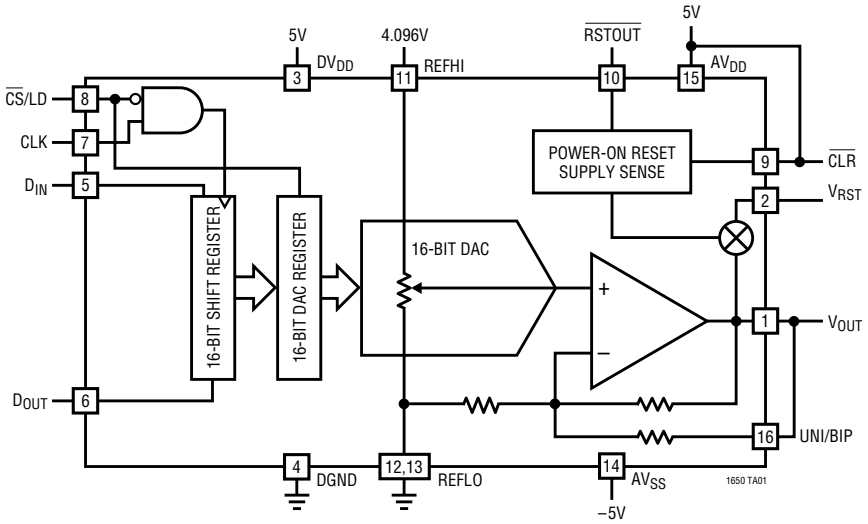


Figure 1. LTC1650 block diagram

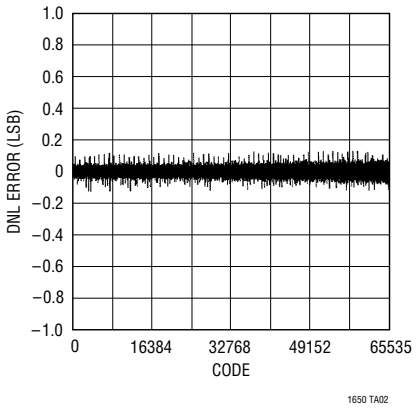


Figure 2. The LTC1650 bipolar output DAC has ±0.3LSB typical DNL.

Component and Measurement Advances Ensure 16-Bit DAC Settling Time (Part Two)

by Jim Williams

Introduction

Reliable measurement of 16-bit DAC settling time is extremely challenging. Part one of this article (in the August 1998 issue of *Linear Technology* magazine) described a method for making this measurement. This second part discusses detailed circuitry and presents results.

Detailed Settling-Time Circuitry

Figure 1 is a detailed schematic of the 16-bit DAC settling-time-measurement circuitry. The input pulse switches all DAC bits simultaneously and is also routed to the oscilloscope via a delay-compensation network. The delay network, composed of CMOS inverters and an adjustable RC network, compensates the oscilloscope's input step signal for the 12ns delay through the circuit's measurement path. The DAC amplifier's output is compared against the LT1236-10V reference via the precision 3k summing resistor ratio set. The LT1236 also furnishes the DAC reference, making the measurement ratiometric. The clamped settle node is unloaded by A1, which drives the sampling bridge. Note the additional clamp diodes at A1's output. These diodes prevent any possibility of abnormal A1 outputs (due to lost supply or supply sequencing anomalies) from damaging the diode array. A3 and associated components tem-

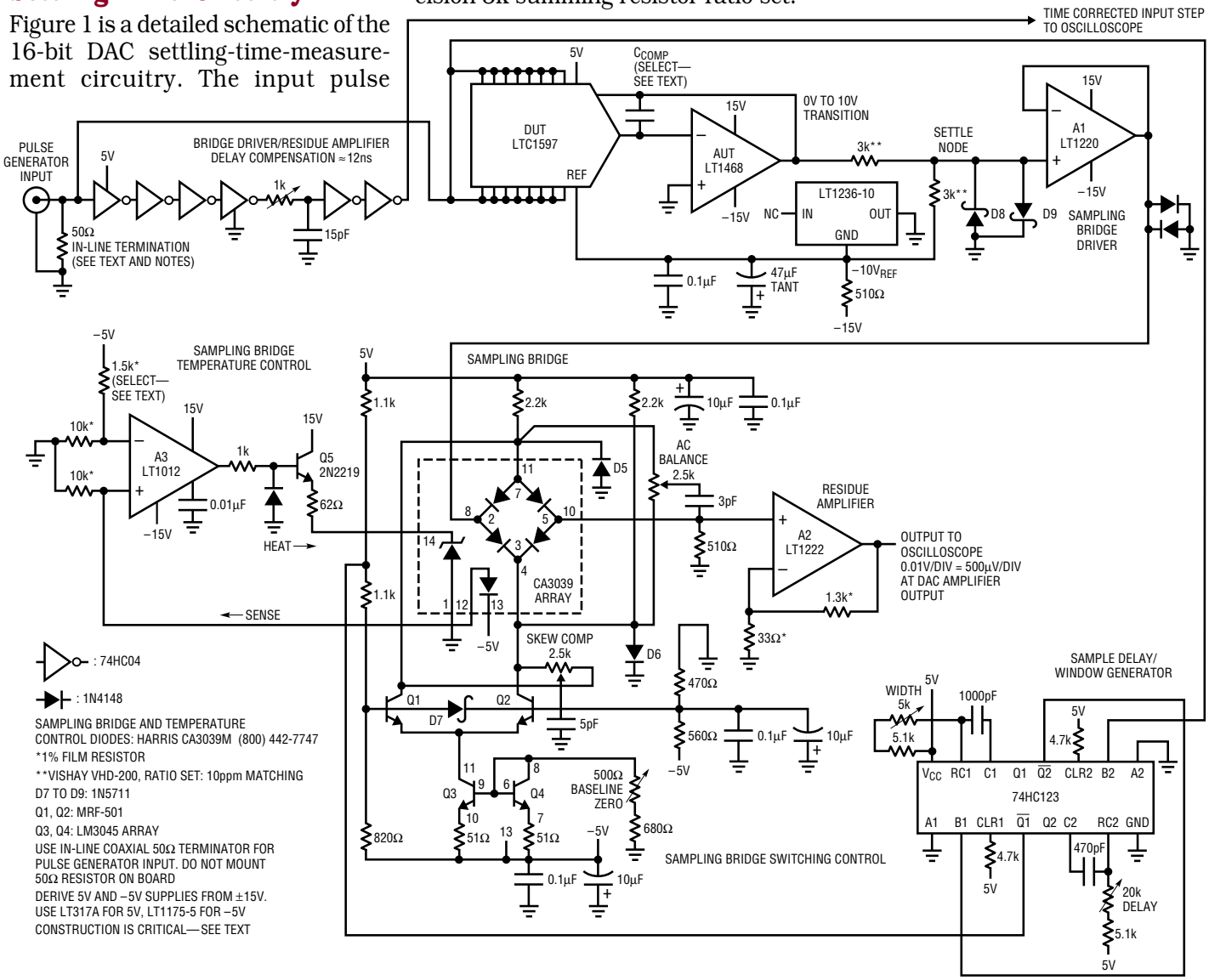


Figure 1. Detailed schematic of DAC-settling-time measurement circuit; optimum performance requires attention to layout.

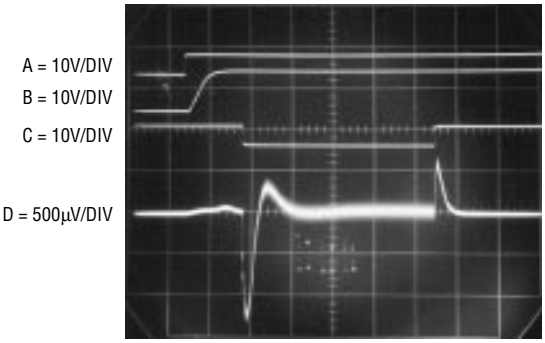


Figure 2. Settling time circuit waveforms include time-corrected input pulse (Trace A), DAC amplifier output (Trace B), sample gate (Trace C) and settling-time output (Trace D). The sample gate window's delay and width are variable.

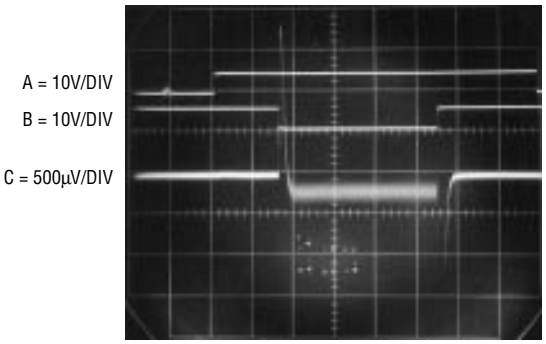


Figure 3. Settling time circuit's output (Trace C) with unadjusted sampling bridge AC and DC trims. The DAC is disabled and the settle node grounded for this test. Excessive switch-drive feedthrough and baseline offset are present. Traces A and B are the input pulse and sample window, respectively.

perature control the sampling diode bridge by comparing a diodes's forward drop to a stable potential derived from the –5V regulator. Another diode, operated in the reverse direction ($V_Z \approx$ 7V) serves as a chip heater. The pin connections shown on the schematic have been selected to provide the best temperature-control performance.

The input pulse triggers the 74HC123 one shot. The one shot is arranged to produce a delayed (controllable by the 20k potentiometer) pulse whose width (controllable by the 5k potentiometer) sets diode bridge on-time. If the delay is set appropriately, the oscilloscope will not see any input until settling is nearly complete, eliminating overdrive. The sample window width is adjusted so that all remaining settling activity is observable. In this way, the oscilloscope's output is reliable and meaningful data may be taken. The one shot's output is level shifted by the Q1–Q4 transistors, providing complementary switching drive to the bridge. The actual switching transistors, Q1–Q2, are UHF types, permitting true differential bridge switching with less than 1ns of time skew.

A2 monitors the bridge output, provides gain and drives the oscilloscope. Figure 2 shows circuit waveforms. Trace A is the input pulse, trace B the DAC amplifier output, trace C the sample gate and trace D the residue amplifier output. When the sample gate goes low, the bridge switches cleanly and the last 1.5mV of slew are easily observed. Ring time is also clearly visible and the amplifier settles nicely to final value. When the sample gate goes high, the bridge switches off, with only 600µV of feedthrough. The 100µV peak before bridge switching (at ≈3.5 vertical divisions) is feedthrough from A1's output, but it is similarly well controlled. Note that there is no off-screen activity at any time—the oscilloscope is never subjected to overdrive.

The circuit requires trimming to achieve this level of performance. The bridge temperature control point is set by grounding Q5's base prior to applying power. Next, apply power and measure A3's positive input with respect to the –5V rail. Select the indicated resistor (1.5k nominal) for a voltage at A3's negative input (again, with respect to –5V) that is 57mV below the positive input's value. Unground Q5's base and the circuit will control the sampling bridge to about 55°C:

$$25°C\ ROOM + \frac{57mV}{1.9mV/°C\ DIODE\ DROP} = 30°C\ RISE = 55°C$$

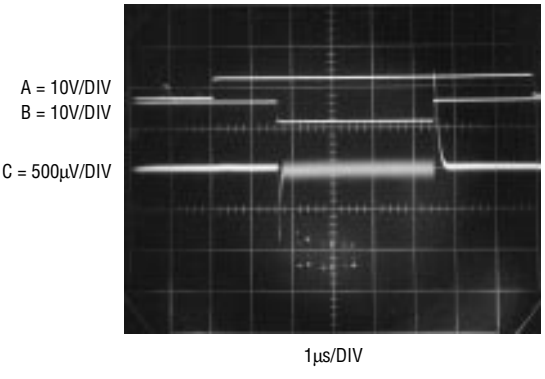


Figure 4. The settling time circuit's output (Trace C) with the sampling bridge trimmed. As in Figure 3, the DAC is disabled and the settle node grounded for this test. Switch drive feedthrough and baseline offset are minimized. Traces A and B are the input pulse and sampling gate, respectively.

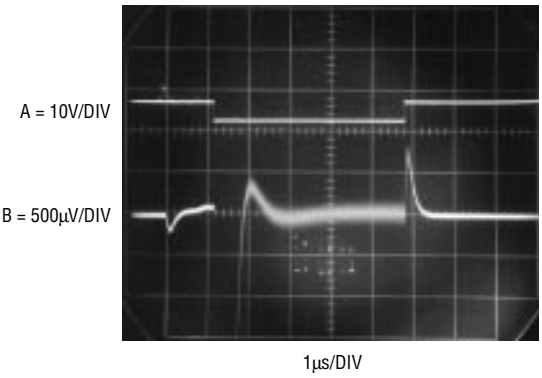


Figure 5. Oscilloscope display with inadequate sample gate delay: the sample window (Trace A) occurs too early, resulting in off-screen activity in the settle output (Trace B). The oscilloscope is overdriven, making displayed information questionable.

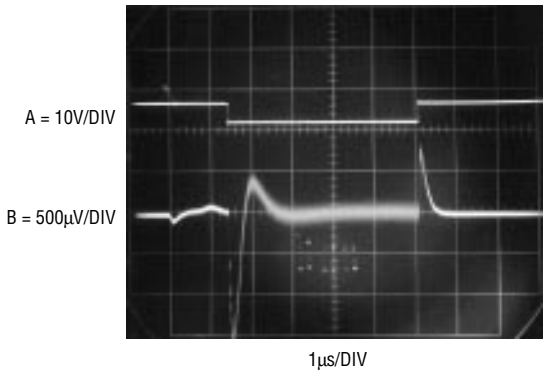


Figure 6. Increasing the sample-gate delay positions the sample window (Trace A) so settle output (Trace B) activity is on-screen.

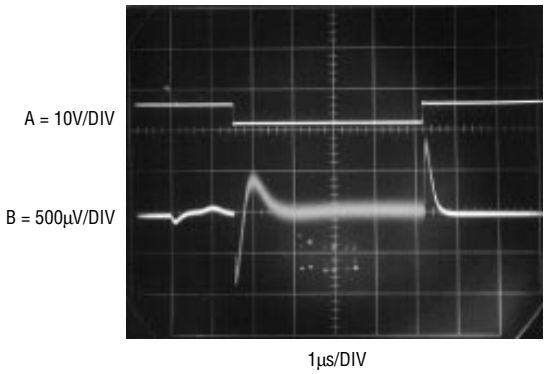


Figure 7. Optimal sample-gate delay positions the sampling window (Trace A) so that all settle output (Trace B) information is well inside screen boundaries.

The DC and AC bridge trims are made once the temperature control is functional. Making these adjustments requires disabling the DAC and amplifier (disconnect the input pulse from the DAC and set all DAC inputs low) and shorting the settle node directly to the ground plane. Figure 3 shows typical results before trimming. Trace A is the input pulse, trace B the sample gate and trace C the residue amplifier output. With the DAC-amplifier disabled and the settle node grounded, the residue amplifier output should (theoretically) always be zero. The photo shows this is not the case for an untrimmed bridge. AC and DC errors are present. The sample gate's transitions cause large, off-screen residue amplifier swings (note residue amplifier's response to the sample gate's turn-off at the ≈8.5 vertical division). Additionally, the residue amplifier output shows significant DC offset error during the sampling interval. Adjusting the AC balance and skew compensation minimizes the switching induced transients. The DC offset is adjusted out with the baseline zero trim. Figure 4 shows the results after making these adjustments. All switching-related activity is now well on-screen and offset error is reduced to unreadable levels. Once this level of performance has been achieved, the circuit is ready for use. Unground the settle node and restore the input pulse connection to the DAC.

Using the Sampling-Based Settling Time Circuit

Figures 5 through 7 underscore the importance of positioning the sampling window properly in time. In Figure 5 the sample gate delay initiates the sample window (trace A) too early and the residue amplifier's output (trace B) overdrives the oscilloscope when sampling commences. Figure 6 is better, with only slight off-screen activity. Figure 7 is optimal. All amplifier residue is well inside the screen boundaries.

In general, it is good practice to "walk" the sampling window up to the last millivolt or so of amplifier slewing so that the onset of ring time is observable. The sampling based approach provides this capability and it is a very powerful measurement tool. Additionally, remember that slower amplifiers may require extended delay and/or sampling window times. This may necessitate larger capacitor values in the 74HC123 one-shot timing networks.

Compensation Capacitor Effects

The DAC amplifier requires frequency compensation to get the best possible settling time. The DAC has appreciable output capacitance, complicating amplifier response and making careful compensation capacitor selection even more important. Figure 8 shows effects of very light compensation.

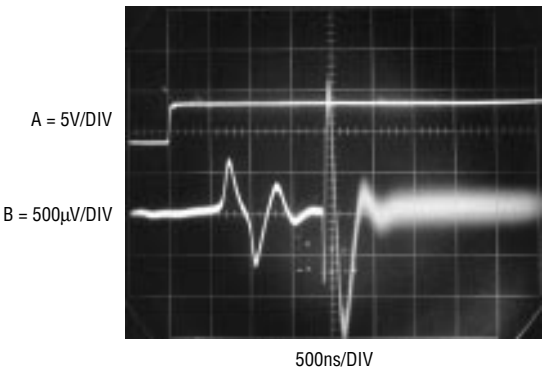


Figure 8. This settling profile with inadequate feedback capacitance shows underdamped response. Excessive ringing feeds through during the sample gate off-period (third through ≈ sixth vertical divisions) but is tolerable (t_{SETTLE} = 2.8μs).

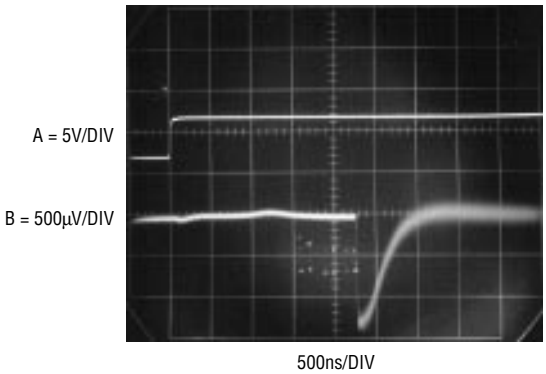


Figure 9. Excessive feedback capacitance overdamps response (t_{SETTLE} = 3.3μs).

Trace A is the time-corrected input pulse and trace B the residue amplifier output. The light compensation permits very fast slewing but excessive ringing amplitude over a protracted time results. The ringing is so severe that it feeds through during a portion of the sample gate off-period, although no overdrive results. When sampling is initiated (just prior to the sixth vertical division) the ringing is seen to be in its final stages, although still offensive. Total settling time is about 2.8µs. Figure 9 presents the opposite extreme. Here, a large value compensation capacitor eliminates all ringing but slows down the amplifier so much that settling stretches out to 3.3µs. The best case appears in Figure 10. This photo was taken with the compensation capacitor carefully chosen for the best possible settling time. Damping is tightly controlled and settling time goes down to 1.7µs.

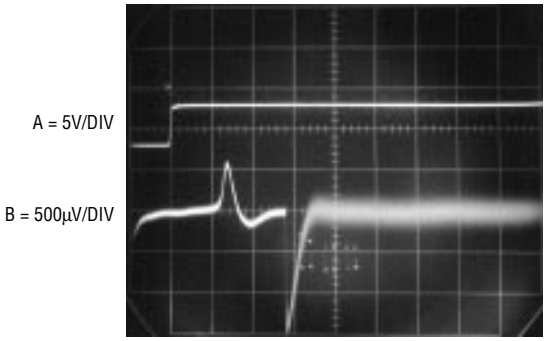


Figure 10. Optimal feedback capacitance yields a tightly damped signature and the best settling time (t_{SETTLE} = 1.7µs).

Settling Times of Various Amplifiers

The previous results, using the LT1468 amplifier, provide extremely fast settling times with high accuracy over temperature. Many applications can tolerate reduced speed, reduced temperature stability or both. Settling times for a number of amplifiers, along with commentary, can be found in LTC Application Note 74, Figure 34. "Optimized" settling times were recorded after individually trimming the feedback capacitors. The "conservative" times represent the worst-case settling times using standard-value compensation capacitors with no trimming.

Conclusion

The sampling-based settling-time circuit appears to be a very useful measurement solution. Expanded discussion and tutorial appear in this article's "root" publication: LTC *Application Note 74, Component and Measurement Advances Ensure 16-Bit DAC Settling Time.*

Net1 and Net2 Serial Interface Chip Set Supports Test Mode

by David Soo

Some serial networks use a test mode to exercise all of the circuits in the interface. The network is divided into local and remote data terminal equipment (DTE) and data-circuit-terminating equipment (DCE), as shown in Figure 1. Once the network is placed in a test mode, the local DTE will transmit on the driver circuits and expect to receive the same signals back from either a local or remote DCE. These tests are called local or remote loopback.

As introduced in the February 1998 issue of *Linear Technology*, the LTC1543/LTC1544/LTC1344A chip set has taken the integrated approach to multiple protocol. By using this chip set, the Net1 and Net2 design work is done. The LTC1545 extends the family by offering test mode capability. By replacing the 6-circuit LTC1544 with the 9-circuit LTC1545, the optional circuits TM (Test Mode), RL (Remote Loopback) and LL (Local Loopback) can now be implemented.

Figure 2 shows a typical application using the LTC1543, LTC1545 and LTC1344A. By just mapping the chip pins to the connector, the design of the interface port is complete. The chip set supports the V.28, V.35, V.36, RS449, EIA-530, EIA-530A or X.21 protocols in either DTE or DCE mode.

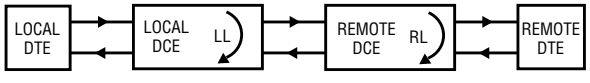


Figure 1. Serial network

Shown here is a DCE mode connection to a DB-25 connector. The mode-select pins, M0, M1 and M2, are used to select the interface protocol, as summarized in Table 1.

Table 1. Mode pin functions

LTC1543/LTC1545 Mode Name	M2	M1	M0
Not Used	0	0	0
EIA-530A	0	0	1
EIA-530	0	1	0
X.21	0	1	1
V.35	1	0	0
RS449/V.36	1	0	1
RS232/V.28	1	1	0
No Cable	1	1	1

SMBus Controlled CCFL Power Supply

by Jim Williams

Figure 1 shows a cold cathode fluorescent lamp (CCFL) power supply that is controlled via the popular SMBus interface. The LT1786 CCFL switching regulator receives the SMBus instruction. The IC converts this instruction to a current, which appears at the I_{OUT} pin. This current, routed to the I_{CCFL} pin, provides a set point for switching regulator operation. The resultant duty cycle at the V_{SW} pin pulls current through L2. L2, acting as a switched current sink, drives a resonant Royer converter composed of Q1–Q2, C1 and L1. The high voltage sine wave produced at L2's secondary drives the floating lamp.

Current flow into the Royer converter is monitored by the IC at pin 13 ("Royer" in Figure 1).[1] Royer current correlates tightly with lamp current, which, in turn, is proportional to intensity. The IC compares the Royer current to the SMBus-derived current, closing a lamp-intensity control loop. The SMBus permits wide-range regulated lamp-intensity control and allows complete IC shutdown. Optimal display and lamp characteristics permit 90% efficiency. The circuit is calibrated by correlating SMBus instruction codes with attendant RMS lamp current. Detailed information on circuit operation and measurement techniques appears in the references below.

References:

1. Williams, Jim. Linear Technology Application Note 65: A Fourth Generation of LCD Backlight Technology. November 1995.
2. LT1786F Data Sheet. Linear Technology Corp. 1998.

[1] Local historians can't be certain, but this may be the only IC pin ever named after a person.

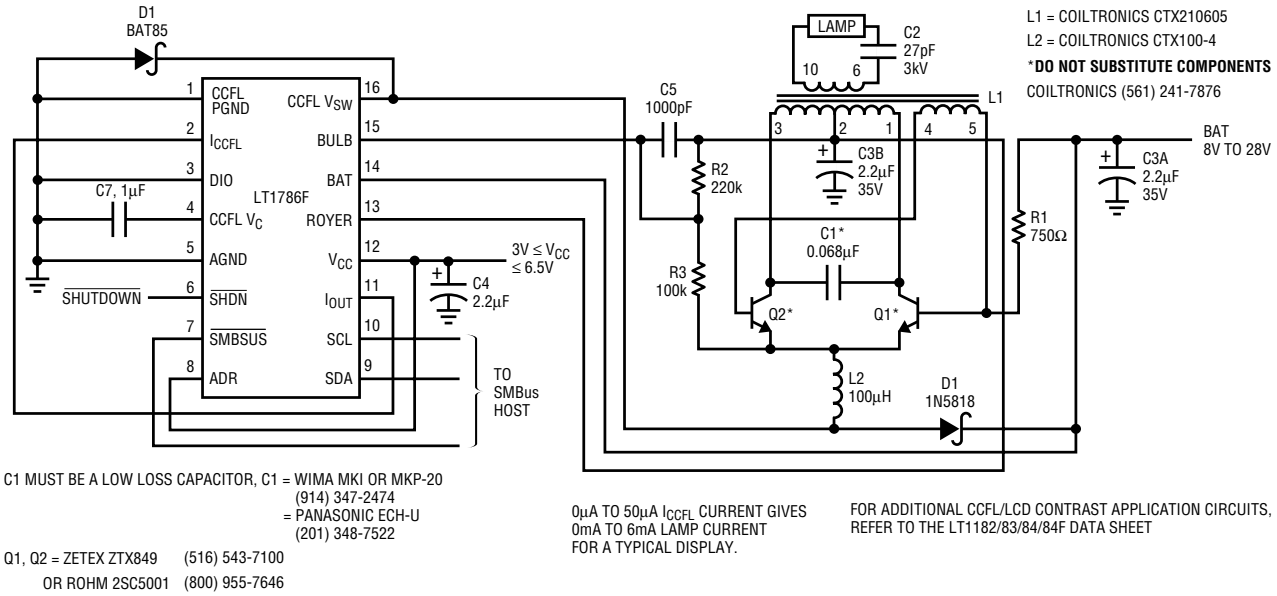


Figure 1. 90% efficient floating CCFL with 2-wire SMBus lamp-current control

Ring Tone, continued from page 29

Analog Inputs Welcome

The scaleable amplification system detailed in Figure 4 can be driven with analog inputs while still maintaining full isolation. Such a system is detailed in Figure 5, where the analog input is filtered (to prevent ailiasing) and converted to PWM. Figure 5 goes on to show the use of an RS485 differential driver to drive a twisted pair line. The receiver end of the twisted pair line is terminated with a resistor and put across the isolation barrier. This provides very good ESD protection on both ends of the line.

Conclusion

The LT1684 is useful in a wide variety of applications. The LT1684 is a highly integrated solution for use in any system that requires digital control of high output voltage or high output power.

Cost and Space Efficient Backlighting for Small LCD Panels

by Jim Williams

A generation of small, portable, "palmtop" computing devices has recently appeared. These products have small LCD displays that use cold cathode fluorescent lamps (CCFLs) for backlighting. These lamps require high voltage AC current drive. Circuitry for this purpose should be physically small, cost effective and electrically efficient.

Figure 1 shows a design that meets the above criteria. The configuration is a current-fed resonant Royer converter driven by an LT1317B micropower switching regulator. The LT1317B effects a switch-mode current sink, supplying the required Royer drive to close a loop at the FB pin. This path includes the lamp and a filter network that rectifies T1's high voltage AC output into DC. In this case, the circuit's operating point, and hence, the lamp current, is set by a potentiometer. Operating-point variation can also be achieved by voltage controlling the optional input, indicated on the schematic.[1] With the components shown, size is about 10mm (W) by 5mm (H) by 40mm (L). The Shutdown pin facilitates circuit turnoff, although removing power from the V_{IN} pin has similar results.

The closed loop operation yields excellent line regulation while ensuring that lamp currents never violate minimum or maximum values. These characteristics allow operation directly from the battery without intensity variation, flicker or shortening of lamp life. Simplicity, low component count, small size and cost effectiveness make this circuit an excellent choice for "palmtop" LCD illumination.

[1] Those finding this description intolerably brief are directed to LTC Application Note 65, where this circuit receives more scholarly attention.

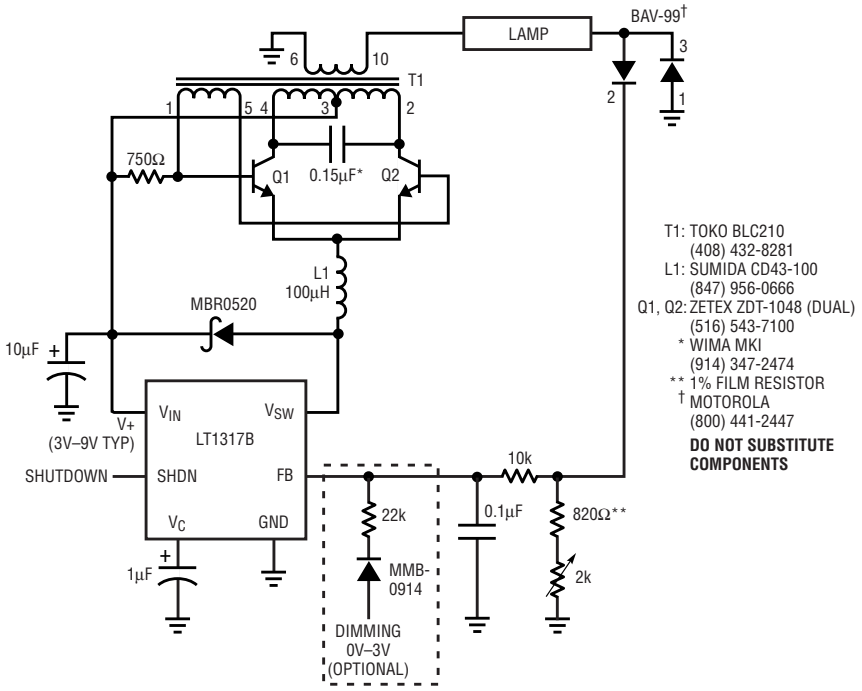


Figure 1. Palmtop computer LCD backlight supply

For more information on parts featured in this issue, see http://www.linear-tech.com/go/ltmag

Bootstrapped Power Supply Permits Single Rail Amplifier Output Swing to Ground (and Below)

by Jim Williams

Many single supply powered applications require amplifier output swings within millivolt or even sub-millivolt levels of ground. Amplifier output saturation limitations normally preclude such operation. Figure 1's power supply bootstrapping scheme achieves the desired characteristics with minimal component addition.

A1, a chopper stabilized amplifier, has a clock output. This output switches Q1, providing drive to the diode-capacitor charge pump. The charge pump output feeds A1's V^- terminal, pulling it below zero, permitting output swing to (and below) ground. If desired, the negative output excursion can be limited by either clamp option shown.

Reliable start-up of this bootstrapped power supply scheme is a valid concern, warranting investigation. In Figure D2, the amplifier's V^- pin (Trace C) initially rises at supply turn-on (Trace A) but heads negative when amplifier clocking (Trace B) commences at about midscreen.

The circuit provides a simple way to obtain output swing to zero volts, permitting a true "live at zero" output.

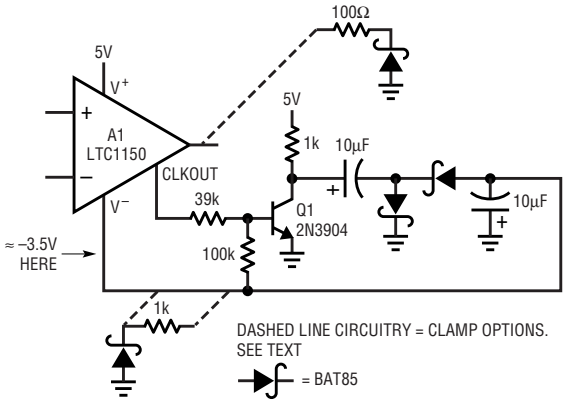


Figure 1. Single rail powered amplifier has true zero volt output swing. A1's clock output switches Q1, driving diode-capacitor charge pump. A1's V^- pin assumes negative voltage, permitting zero (and below) volt output swing.

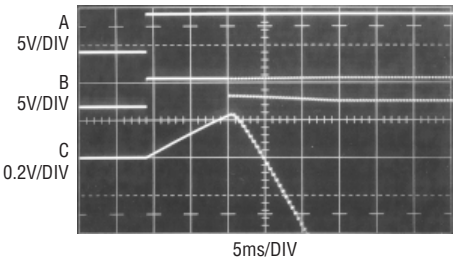


Figure 2. Amplifier bootstrapped supply start-up. Amplifier V^- pin (trace C) initially rises positive at 5V supply (trace A) turn-on. When amplifier internal clock starts (trace B, 5th vertical division), charge pump activates, pulling V^- pin negative.

LTC3439, continued from page 35

20µA. The $\overline{SHDN}$ pin can easily be configured to provide a supply undervoltage lockout (UVLO) function.

Protection features include current limiting, which facilitates startup into a high capacitance load; and cross conduction prevention circuitry, which keeps the two switches from being on simultaneously.

The LT3439 is available in a thermally enhanced 16-pin TSSOP with exposed underside metal.

Low Noise Step-up Converter Produces ±15V at 100mA from a 5V Input

Figure 1 shows a design that provides regulated ±15V at 100mA outputs from a 5V±5% input. Output ripple is less than 150µV or 0.001% of V_{OUT} measured at full load. Efficiency of the supply is approximately 71% measured at full load.

The LT1964-BYP and the LT1761-BYP linear regulators regulate the output to within 0.1% of nominal over the full line and load range.

Conclusion

The LT3439 DC Transformer Driver greatly simplifies the design of efficient low noise isolated power supplies. By reducing a major source of the EMI with voltage and current slew control, designs using the LT3439 avoid expensive shielding and filtering requirements and save the cost and time incurred by multiple iterative layouts.

For more information on parts featured in this issue, see http://www.linear.com/go/ltmag

Determine the Real Internal Resistance of a Battery

by Jim Williams

Introduction

An accurate measure of a battery's true internal resistance can reveal much about its condition or its suitability for an application, but measurement is not as easy as hooking up a precision ohmmeter. Inherent capacitance of a battery reduces the accuracy of measurements taken with a common AC-based milliohmmeters operating in the kHz range. Figure 1, a very simplistic battery model, shows a resistive divider with a partial shunt capacitive term. This capacitive term introduces error in AC based measurement. Also, the battery's unloaded internal resistance can significantly differ from its loaded value. A realistic determination of internal resistance must be made under loaded conditions at or near DC.

Figure 2's circuit meets these requirements, permitting accurate internal resistance determination of batteries up to 13V over a range of 0.001Ω to 1.000Ω. A1, Q1 and associated components form a closed loop current sink which loads the battery via Q1's drain. The 1N5821 provides reverse battery protection.

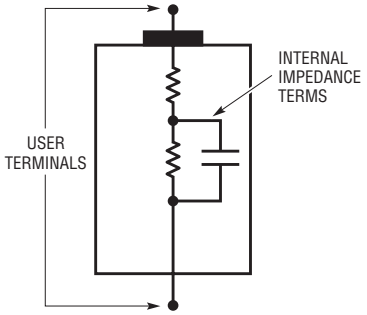


Figure 1. Simplistic model shows battery impedance terms include resistive and capacitive elements. Capacitive component corrupts AC based measurement attempts to determine internal DC resistance. More realistic results occur if battery voltage drop is measured under known load.

The voltage across the 0.1Ω resistor, and hence the battery load, is determined by A1's "+" input voltage. This potential is alternately switched, via S1, between 0.110V and 0.010V derived from the 2.5V reference driven 3-resistor string. S1's 0.5Hz square wave switching drive comes from the CD4040 frequency divider. The result of this action is a 100mA biased, 1A, 0.5Hz square wave load applied to the battery. The battery's internal resistance causes a 0.5Hz amplitude modulated square wave to appear at the Kelvin-sensed, S2-S3-A2 synchronous demodulator. The demodulator DC output is buffered by chopper stabilized A2, which provides the circuit output. A2's internal 1 kHz clock, level shifted by Q2, drives the CD4040 frequency divider. One divider output supplies the 0.5Hz square wave; a second 500Hz output activates a charge pump, providing a –7V potential to A2. This arrangement allows A2's output to swing all the way to zero volts.

The circuit pulls 230µA from its 9V battery power supply, permitting about 3000 hours battery life. Other specifications include operation down to 4V with less than 1mV (0.001Ω) output variation, 3% accuracy and battery-under-test range of 0.9V–13V. Finally, note that battery discharge current and repetition rate are easily varied from the values given, permitting observation of battery resistance under a variety of conditions.

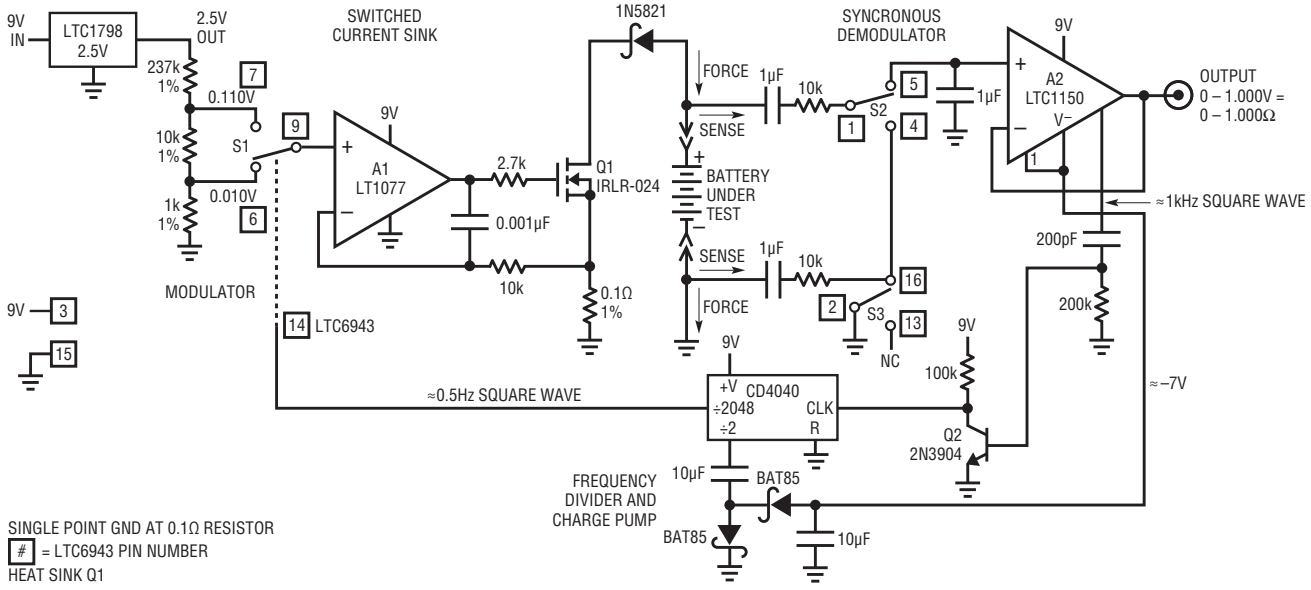


Figure 2. Battery internal resistance is determined by repetitively stepping calibrated discharge current and reading resultant voltage drop. S1 based modulator, clocked from frequency divider, combines with A1-Q1 switched current sink to generate stepped, 1A battery discharge cycles. S2-S3-A2 synchronous demodulator extracts modulated voltage drop information, provides DC output calibrated in Ohms.

40nV$_{P-P}$ Noise, 0.05µV/°C Drift, Chopped FET Amplifier

by Jim Williams

Figure 1's circuit combines the 5V rail-to-rail performance of the LTC6241 with a pair of extremely low noise JFETs configured in a chopper based carrier modulation scheme to achieve extraordinarily low noise and DC drift. This circuit's performance suits the demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

The LTC1799's output is divided down to form a 2-phase 925Hz square wave clock. This frequency, harmonically unrelated to 60Hz, provides excellent immunity to harmonic beating or mixing effects which could cause instabilities. S1 and S2 receive complementary drive, causing the A1-based stage to see a chopped version of the input voltage. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to DC output amplifier A2. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. Because the input stage is AC coupled, its DC errors do not affect overall circuit characteristics, resulting in the extremely low offset and drift noted.

Figure 2, noise measured over a 50 second interval, shows 40nV in a 0.1Hz to 10Hz bandwidth. This low noise is attributed to the input JFET's die size and current density.

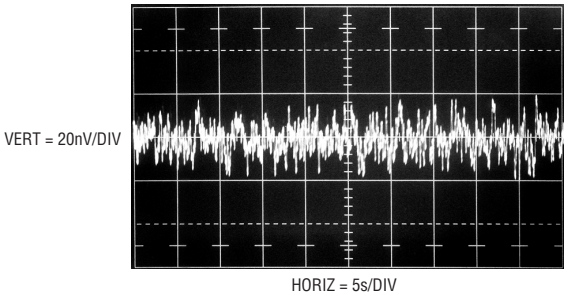


Figure 2. Noise measures 40nV$_{P-P}$ in 50s sample period

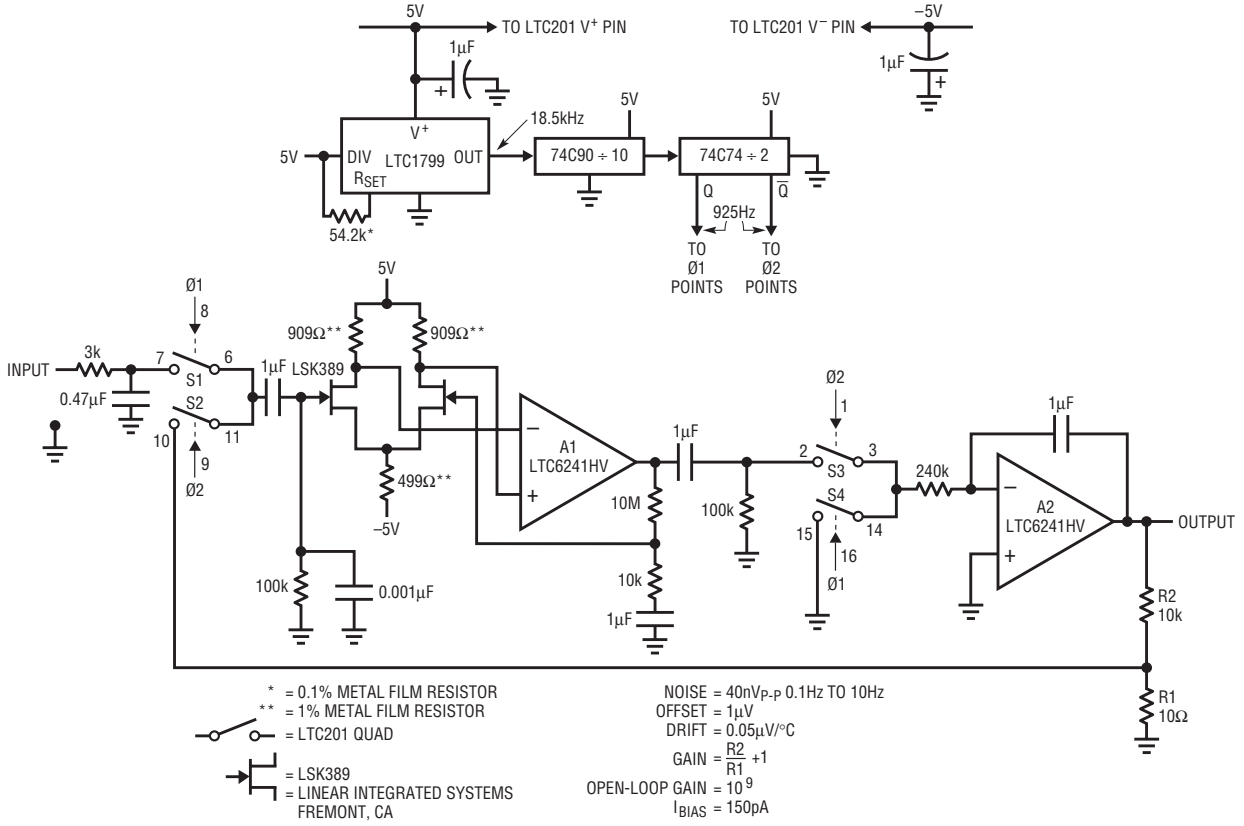


Figure 1. 40nV noise chopper amplifier

J-FET-Based DC/DC Converter Starts and Runs from 300mV Supply

by Jim Williams

A J-FET's self-biasing characteristic can be utilized to construct a DC/DC converter powered from as little as 300mV. Solar cells, thermopiles and single stage fuel cells, all with outputs below 600mV, are typical power sources for such a converter.

Figure 1, an N-channel J-FET I-V plot, shows drain-source conduction under zero bias (gate and source tied together) conditions. This property can be exploited to produce a self-starting DC/DC converter that runs from 0.3V to 1.6V inputs.

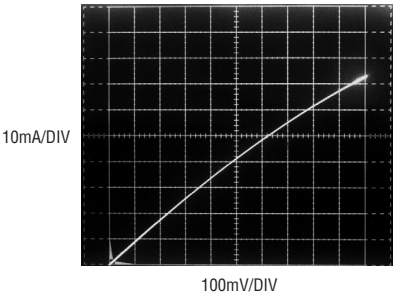


Figure 1. Zero volt biased JFET I-V curve shows 10mA conduction at 100mV, rising above 40mA at 500mV. Characteristic enables construction of DC/DC converter powered from 300mV supply.

Figure 2 shows the circuit. Q1 and T1 form an oscillator with T1's secondary providing regenerative feedback to Q1's gate. When power is applied, Q1's gate is at zero volts and its drain conducts current via T1's primary. T1's phase inverting secondary responds by going negative at Q1's gate, turning it off. T1's primary current ceases, its secondary collapses and oscillation commences. T1's primary action causes positive going "flyback" events at Q1's drain, which are rectified and filtered. Q2's approximately 2V turn-on potential isolates the load, aiding start-up. When Q2 turns on, circuit output heads towards 5V. C1, powered from Q2's source, enforces output regulation by comparing a portion of the output with its internal voltage reference. C1's switched output controls Q1's on-time via Q3, forming a control loop.

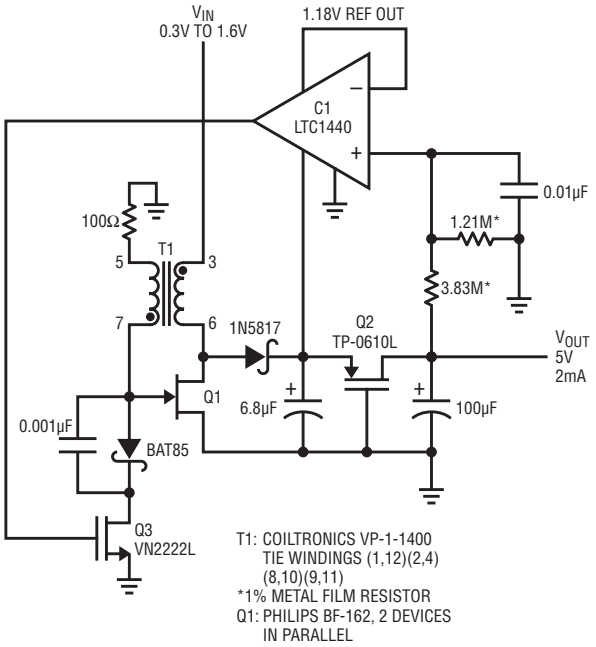


Figure 2. J-FET based DC/DC converter runs from 300mV input. Q1-T1 oscillator output is rectified and filtered. Load is isolated until Q2 source arrives at approximately 2V, aiding start-up. Comparator and Q3 close loop around oscillator, controlling Q1's on-time to stabilize 5V output.

Waveforms for the circuit include the AC coupled output (Figure 3, trace A), C1's output (trace B) and Q1's drain flyback events (trace C). When the output drops below 5V, C1 goes low, turning on Q1. Q1's resultant flyback events continue until the 5V output is restored. This pattern repeats, maintaining the output.

The 5V output can supply up to 2mA, sufficient to power circuitry or supply bias to a higher power switching regulator when more current is required. The circuit will start into loads of 300µA at 300mV input; 2mA loading requires a 475mV supply. Figure 4 plots minimum input voltage vs output current over a range of loads.

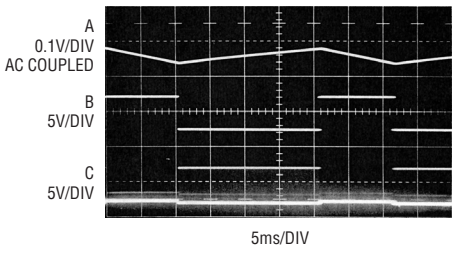


Figure 3. J-FET based DC/DC converter waveforms. When supply output (trace A) decays, C1 (trace B) switches, allowing Q1 to oscillate. Resultant flyback events at Q1 drain (trace C) restore supply output.

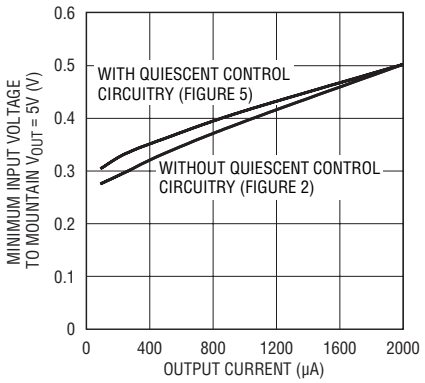


Figure 4. J-FET based DC/DC converter of Figure 2 starts and runs into 100µA load at V_{IN} = 275mV. Regulation to 2mA is possible, although required V_{IN} rises to 500mV. Quiescent current control circuitry of Figure 5 slightly increases input voltage required to support load at V_{IN} < 500mV.

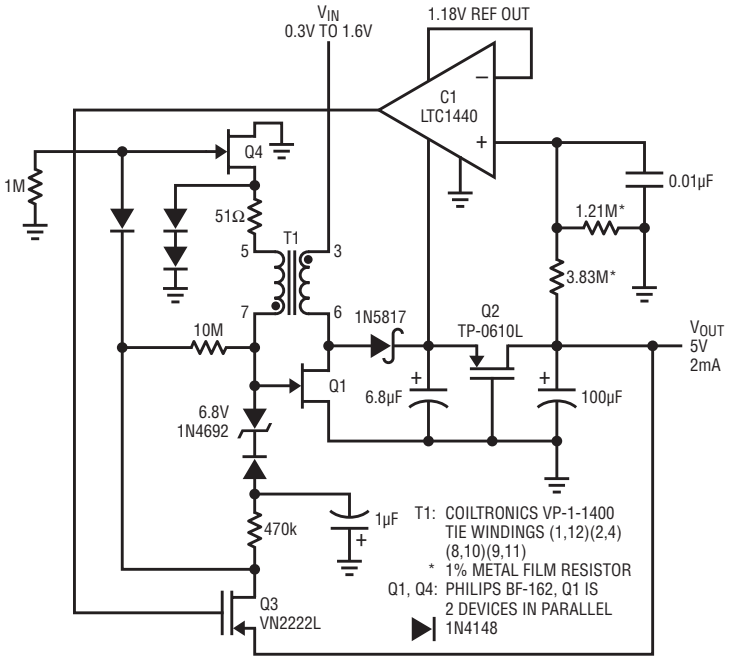


Figure 5. Adding Q3, Q4 and bootstrapped negative bias generator reduces quiescent current. Comparator directed Q3 switches Q4, more efficiently controlling Q1's gate drive. Q2 and zener diode isolate all loading during Q1 start-up.

Q3's shunt control of Q1 is simple and effective, but results in a 25mA quiescent current drain. Figure 5's modifications reduce this figure to 1mA by series switching T1's secondary. Here, Q3 switches series-connected Q4, more efficiently controlling Q1's gate drive. Negative turn-off bias for Q4 is bootstrapped from T1's secondary; the 6.8V zener holds off bias supply loading during initial power application, aiding start-up. Figure 4 shows minimal penalty imposed by the added quiescent current control circuitry.

LT3487, continued from page 13

until the positive side reaches 87% of its final voltage. The output disconnect is also designed so that both channels can collapse together gently when the chip is shut down.

Output Disconnect

In a standard boost regulator, the inductor and Schottky diode provide a DC current path from the input to the output, even when the regulator is shut down. Any load at the output when the chip is shut down can continue to drain the V_{IN} source. The LT3487 addresses this issue with an on-chip output disconnect. The output disconnect is a PNP pass transistor that eliminates the DC loss path. The pass transistor is controlled by a circuit that varies its base current to keep it at the edge of saturation, yielding the best compromise between voltage drop across the PNP and quiescent current. The disconnect in the LT3487 can support loads of 50mA with a V_{CE} of less than 210mV.

V_{BAT} Pin

The V_{BAT} pin is an innovation that allows output disconnect operation in a wide range of applications. V_{BAT} monitors the voltage at the input of the boost inductor and allows the positive output to stay active until the CAP node falls to 1.2V above V_{BAT}. This ensures that output disconnect continues operating even after the part goes into shutdown. Since output disconnect continues to work, the positive output doesn't fall sharply to ground before the negative bias discharges. The V_{BAT} pin allows the inductors to be powered from a different source than V_{IN} while still maintaining the disconnect operation. This can be useful in a system using a 2-cell supply where a low voltage boost provides 3.3V for the V_{IN} supply. By connecting V_{BAT} as well as the inductors to the 2-cell supply, the positive output is able to stay on as long as possible when the part goes into shutdown.

Applications

The LT3487 can be used in a CCD bias as well as other applications that require a positive and negative bias such as ±12V data acquisition systems. The boost channel can produce voltages up to 30V as long as the part can meet the required duty cycle. Similarly, the inverting channel can produce voltages down to –30V. This high voltage capability allows the LT3487 to be used in many LCD applications.

Conclusion

The LT3487 simplifies and shrinks CCD bias supplies without compromising on performance or features. The soft-start and output disconnect features ensure that the input battery doesn't encounter current spikes or shutdown leakage. The high current capability satiates even the most power-hungry video applications.

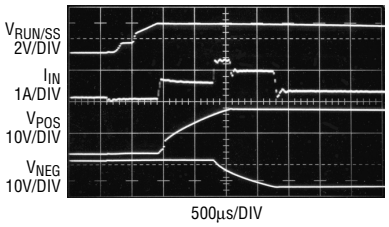


Figure 3. Startup without soft-start capacitor

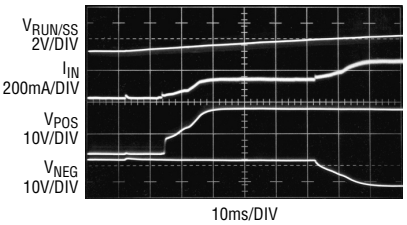


Figure 4. Startup with 100nF soft-start capacitor

Sub-µA RMS Current Measurement for Quartz Crystals

by Jim Williams

Quartz crystal RMS operating current is critical to long-term stability, temperature coefficient and reliability. Accurate determination of RMS crystal current, especially in micropower types, is complicated by the necessity to minimize introduced parasitics, particulary capacitance, which corrupt crystal operation.

Figure 1's high gain, low noise amplifier combines with a commercially available closed core current probe to permit the measurement. An RMS-to-DC converter supplies the RMS value. The quartz crystal test circuit shown in dashed lines exemplifies a typical measurement situation. The Tektronix CT-1 current probe monitors crystal current while introducing minimal parasitic loading. The probe's 50Ω terminated output is fed to A1. A1 and A2 take a closed loop gain of 1120; excess gain over a nominal gain of 1000 corrects for the CT-1's 12% low frequency gain error at 32.768kHz.[1] A3 and A4 contribute a gain of 200, resulting in total amplifier gain of 224,000. This figure results in a 1V/µA scale factor at A4 referred to the gain corrected CT-1's output. A4's LTC1563-2 bandpass filtered output feeds an LTC1968-based RMS-to-DC converter (A5), which provides the circuit's output. The signal processing path constitutes an extremely narrow band amplifier tuned to the crystal's

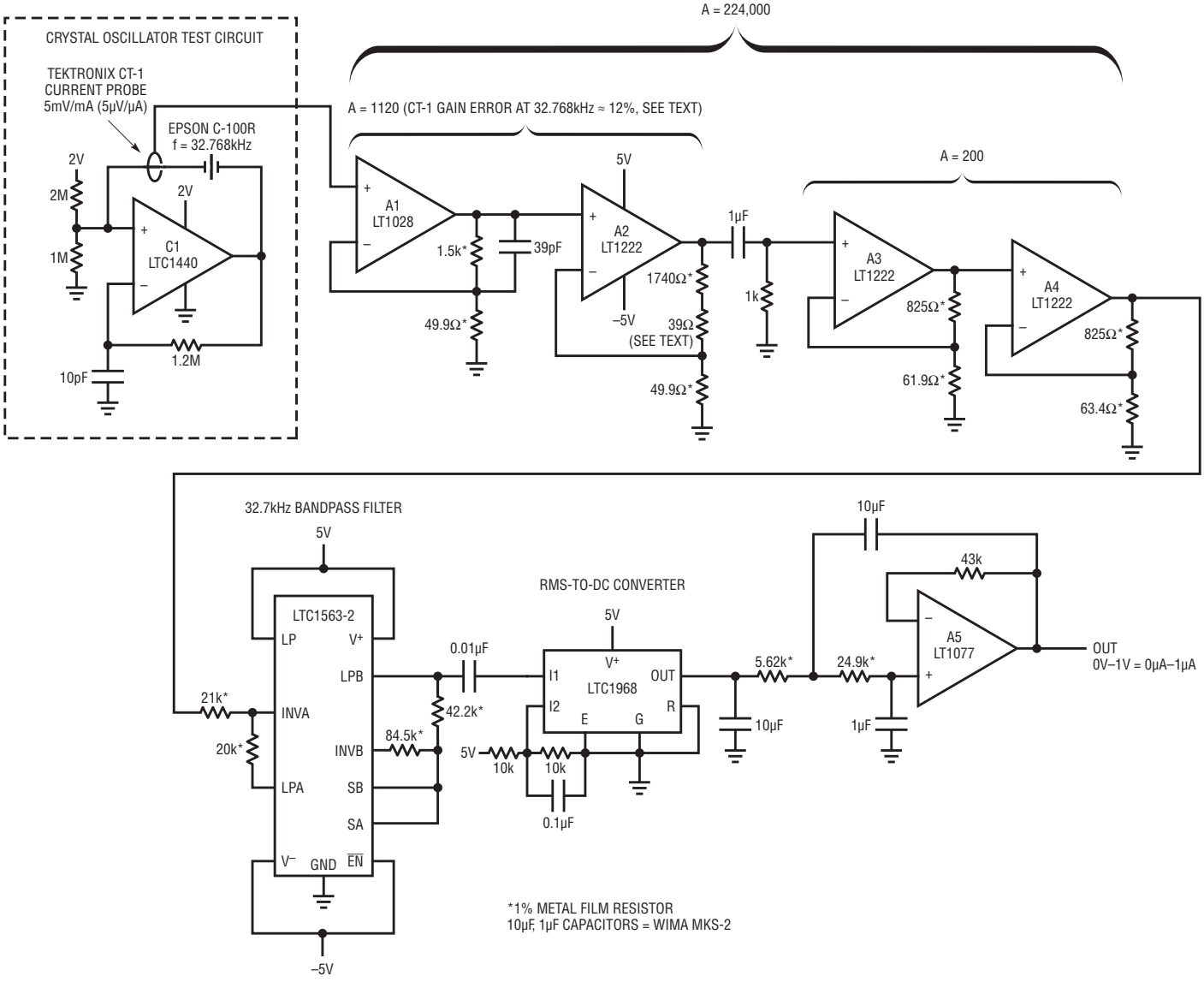


Figure 1. Op amps A1–A4 furnish gain of > 200,000, permitting sub-µA crystal current measurement. The LTC1563-2 bandpass filter smooths residual noise while providing unity gain at 32.768kHz. The LTC1968 RMS-to-DC converter supplies RMS calibrated output.

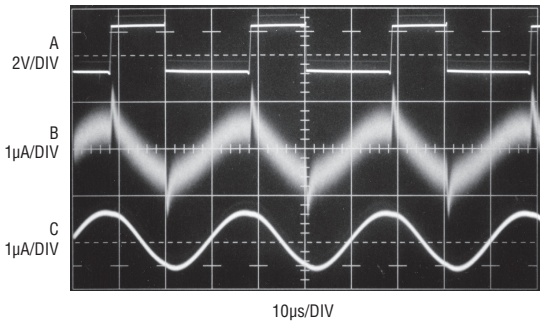


Figure 2. The 32.768kHz output of the crystal oscillator (Trace A) and crystal current monitored at A4 output (Trace B) and the RMS-to-DC converter input (Trace C). Peaks in Trace B's unfiltered waveform derive from inherent and parasitic paths shunting the crystal.

frequency. Figure 2 shows typical circuit waveforms. Crystal drive, taken at C1's output (trace A), causes a 530nA RMS crystal current, which is represented at A4's output (Trace B) and the RMS-to-DC converter input (Trace C). Peaking visible in Trace B's unfiltered presentation derive from inherent and parasitic paths shunting crystal.

Typical circuit accuracy is 5%. Uncertainty terms include the transformer's tolerances, its approximately 1.5pF loading and resistor/RMS-to-DC converter error. Calibrating the circuit reduces error to less than 1%. Calibration involves driving the transformer with 1µA at 32.7kHz. This is facilitated by biasing a 100k, 0.1% resistor with an oscillator set at 0.1V output. The output voltage should be verified with an RMS voltmeter having appropriate accuracy. Figure 1 is calibrated by padding A2's gain with a small resistive correction, typically 39Ω. LT

Notes

1 The validity of this gain error correction at one sinusoidal frequency—32.768kHz—was investigated with a 7-sample group of Tektronix CT-1s. Device outputs were collectively within 0.5% of 12% down for a 1.00µA, 32.768kHz sinusoidal input current. Although this tends to support the measurement scheme, it is worth noting that these results are as measured. Tektronix does not guarantee performance below the specified –3dB, 25kHz low frequency roll-off.

New Device Cameos

High Voltage Dual Input Li-Ion Battery Charger

The LTC4075HVX is a standalone linear charger that is capable of charging a single-cell Li-Ion/Polymer battery from both wall adapter and USB inputs. The charger can detect power at the inputs and automatically select the appropriate power source for charging.

No external sense resistor or blocking diode is required for charging due to the internal MOSFET architecture. The LTC4075HVX features a maximum 22V rating for both wall adapter and USB inputs although charging stops if the selected power source exceeds the overvoltage limit (typical 6V). Internal thermal feedback regulates the battery charge current to maintain a constant die temperature during high power operation or high ambient temperature conditions. The float voltage is fixed at 4.2V and the charge current is programmed with an external resistor. The LTC4075HVX terminates the charge cycle when the charge current drops below the programmed termination threshold after the final float voltage is reached.

Other features include automatic recharge, undervoltage lockout, charge status outputs, and "power present" status outputs to indicate the presence of wall adapter or USB power. No trickle charge allows full current from the charger when a load is connected directly to the battery.

Small 1.8A Step-Down Regulator Switches at 4MHz for Space-Sensitive Applications

The LTC3568 is a 10-lead DFN, synchronous, step-down, current mode, DC/DC converter, intended for medium power applications. It operates within a 2.5V to 5.5V input voltage range and switches at up to 4MHz, making it possible to use tiny capacitors and inductors that are under 1mm in height. The output of the LTC3568 is adjustable from 0.8V to 5V, and its 0.11Ω switches allows up to 1.8A of output current at high efficiency. By using the LTC3568 in a small 3mm × 3mm, 10-lead DFN package, a complete DC/DC converter can consume less than 0.3 square inches of board real estate.

Efficiency is extremely important in battery-powered applications, and the LTC3568 keeps efficiency high with an automatic, power saving Burst Mode operation, which reduces gate charge losses at low load currents. With no load, the part only draws 60µA, and in shutdown, the device draws less than 1µA, making it ideal for low current applications.

The LTC3568 uses a current-mode, constant frequency architecture that benefits noise sensitive applications. Burst Mode operation is an efficient solution for low current applications, but sometimes noise suppression is a priority. To reduce noise problems, a pulse-skipping mode and a forced continuous mode are available, which decreases the ripple noise at low currents. Although not as efficient as Burst Mode operation at low currents, pulse-skipping mode and forced continuous mode still provide high efficiency for moderate loads. In dropout, the internal P-channel MOSFET switch is turned on continuously, thereby maximizing the usable battery life.

A Power Good output is available for power supply monitoring or for Power On Reset use. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output voltages are not within about ±7.5%.

The LTC3568's small size, high efficiency, low component count and flexibility make it an ideal DC/DC converter for portable devices. LT

Diode Turn-On Time Induced Failures in Switching Regulators

Never Has So Much Trouble Been Had by So Many with So Few Terminals

by Jim Williams and David Beebe

This article is excerpted from the Linear Technology Application Note AN122 with the same title.

Introduction

Most circuit designers are familiar with diode dynamic characteristics such as charge storage, voltage dependent capacitance and reverse recovery time. Less commonly acknowledged and manufacturer specified is diode forward turn-on time. This parameter describes the time required for a diode to turn on and clamp at its forward voltage drop. Historically, this extremely short time, units of nanoseconds, has been so small that user and vendor alike have essentially ignored it. It is rarely discussed and almost never specified. Recently, switching regulator clock rate and transition time have become faster, making diode turn-on time a critical issue. Increased clock rates are mandated to achieve smaller magnetics size; decreased transition times somewhat aid overall efficiency but are principally needed to minimize IC heat rise. At clock speeds beyond about 1MHz, transition time losses are the primary source of die heating.

A potential difficulty due to diode turn-on time is that the resultant transitory "overshoot" voltage across the diode, even when restricted to nanoseconds, can induce overvoltage stress, causing switching regulator IC failure. As such, careful testing is required to qualify a given diode for a particular application to insure reliability. This testing, which assumes low loss surrounding components and layout in the final application, measures turn-on overshoot voltage due to diode parasitics only. Improper associated component selection and layout will contribute additional overstress terms.

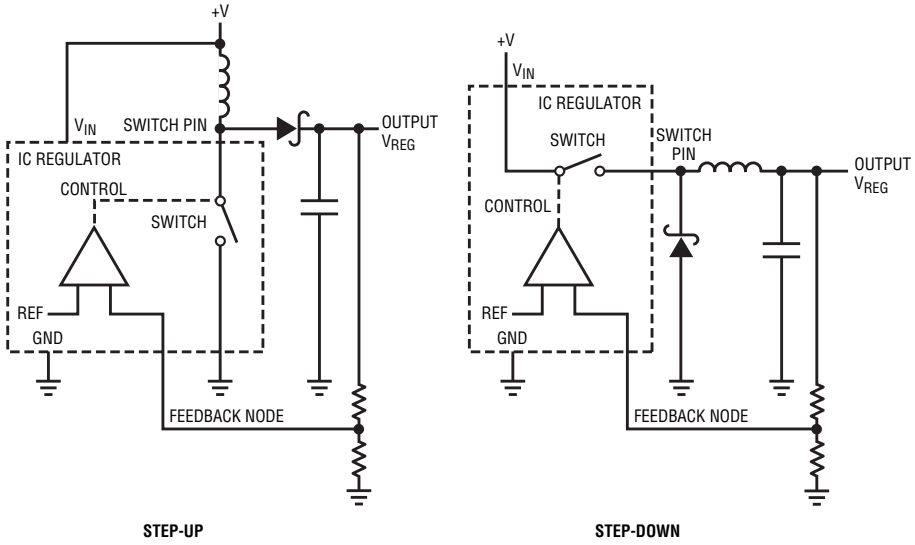


Figure 1. Typical voltage step-up/step-down converters. Assumption is diode clamps switch pin voltage excursion to safe limits.

Diode Turn-On Time Perspectives

Figure 1 shows typical step-up and step-down voltage converters. In both cases, the assumption is that the diode clamps switch pin voltage excursions to safe limits. In the step-up case, this limit is defined by the switch pins

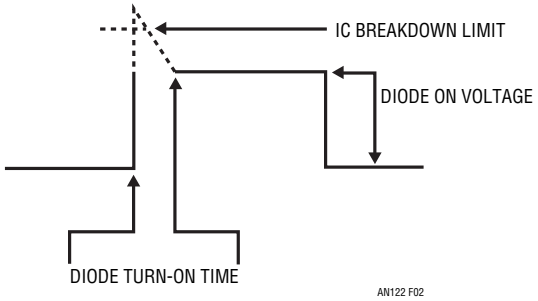


Figure 2. Diode forward turn-on time permits transient excursion above nominal diode clamp voltage, potentially exceeding IC breakdown limit.

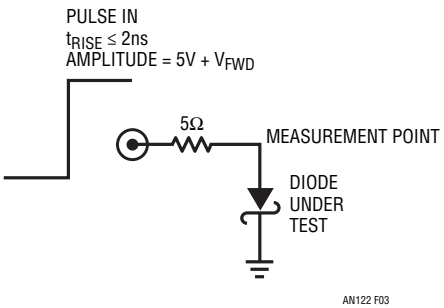


Figure 3. Conceptual method tests diode turn-on time at 1A. Input step must have exceptionally fast, high fidelity transition.

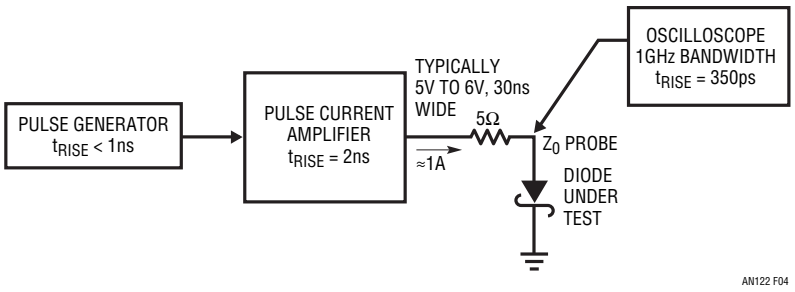


Figure 4. Detailed measurement scheme indicates necessary performance parameters for various elements. Subnanosecond rise time pulse generator, 1A, 2ns rise time amplifier and 1GHz oscilloscope are required.

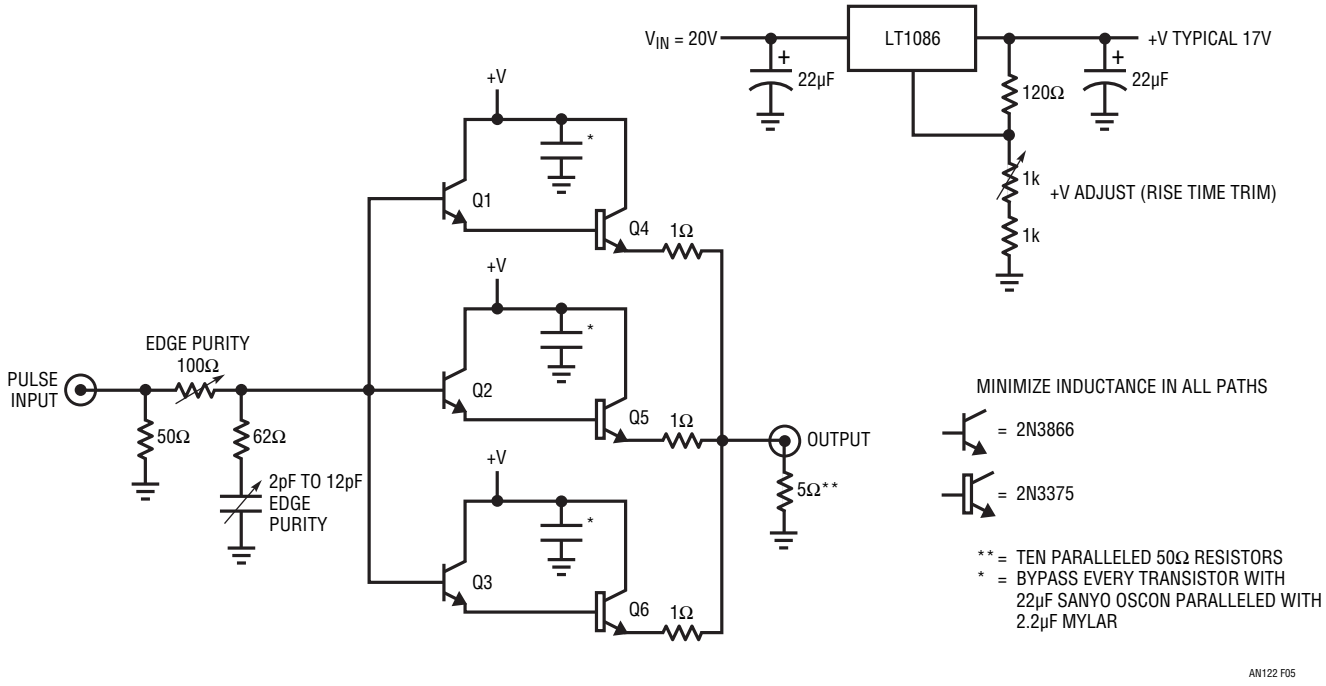


Figure 5. Pulse amplifier includes paralleled, darlington driven RF transistor output stage. Collector voltage adjustment ("rise time trim") peaks Q4 to Q6 F_T, input RC network optimizes output pulse purity. Low inductance layout is mandatory.

maximum allowable forward voltage. The step-down case limit is set by the switch pins maximum allowable reverse voltage.

Figure 2 indicates the diode requires a finite length of time to clamp at its forward voltage. This forward turn-on time permits transient excursions above the nominal diode clamp voltage, potentially exceeding the IC's breakdown limit. The turn-on time is typically measured in nanoseconds, making observation difficult. A further complication is that the turn-on overshoot occurs at the amplitude extreme of a pulse waveform, precluding high resolution amplitude measurement. These factors must be considered when designing a diode turn-on test method.

Figure 3 shows a conceptual method for testing diode turn-on time. Here, the test is performed at 1A although other currents could be used. A pulse steps 1A into the diode under test via the 5Ω resistor. Turn-on time voltage excursion is measured directly at the diode under test. The figure

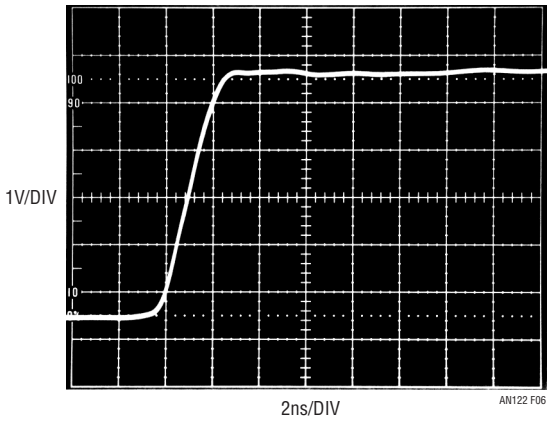


Figure 6. Pulse amplifier output into 5Ω. Rise time is 2ns with minimal pulse-top aberrations.

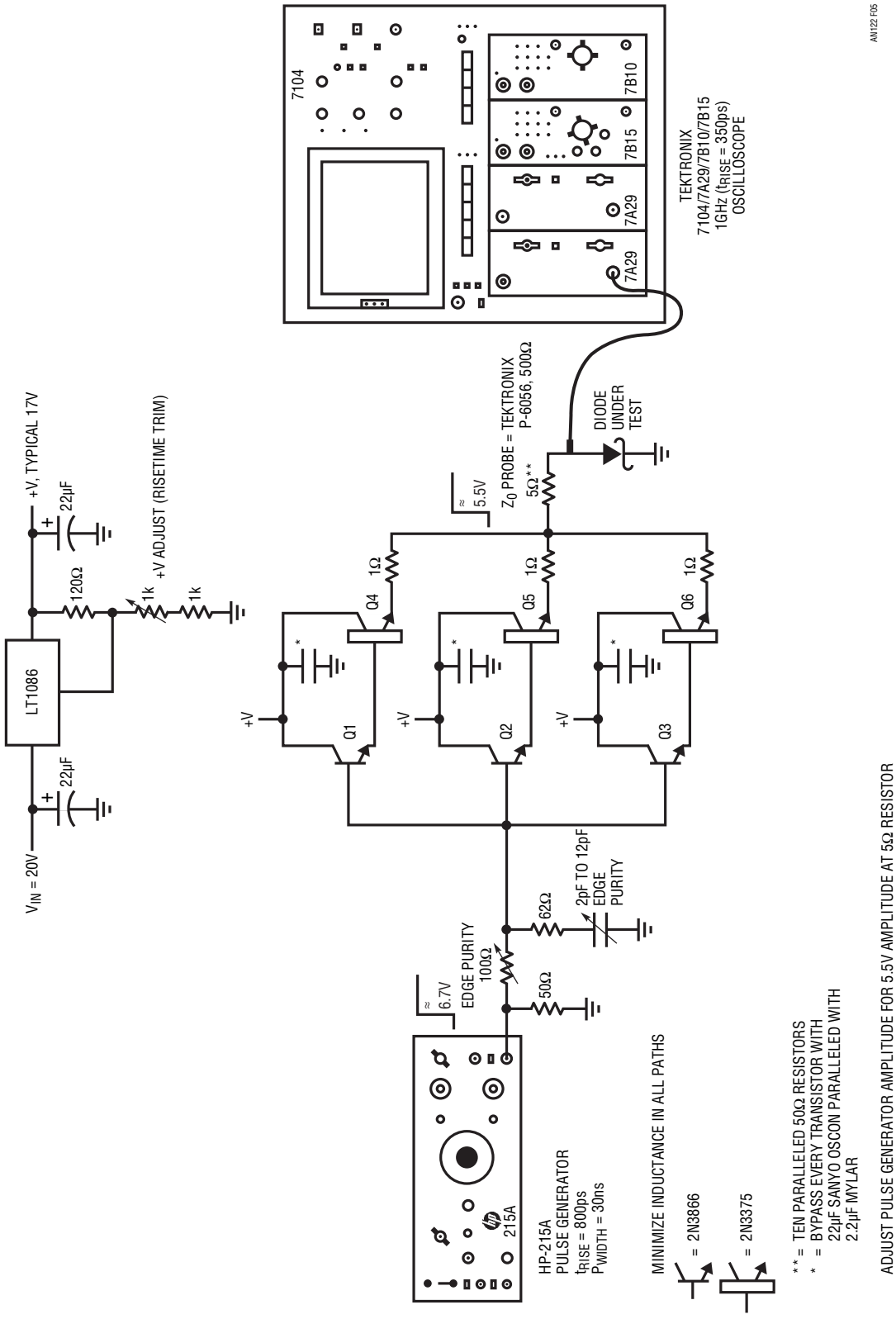


Figure 7. Complete diode forward turn-on time measurement arrangement includes subnanosecond rise time pulse generator, pulse amplifier, Z0 probe and 1GHz oscilloscope.

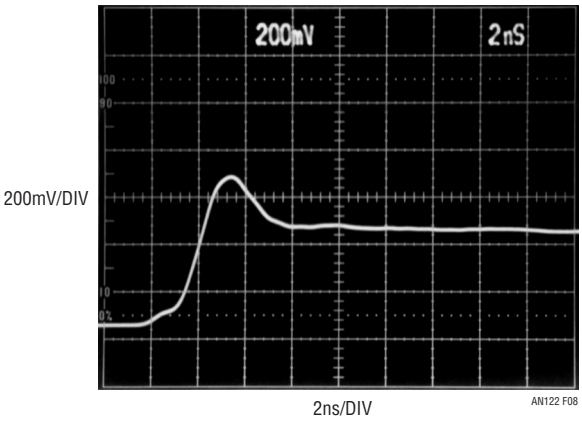


Figure 8. "Diode Number 1" overshoots steady state forward voltage for ≈3.6ns, peaking 200mV.

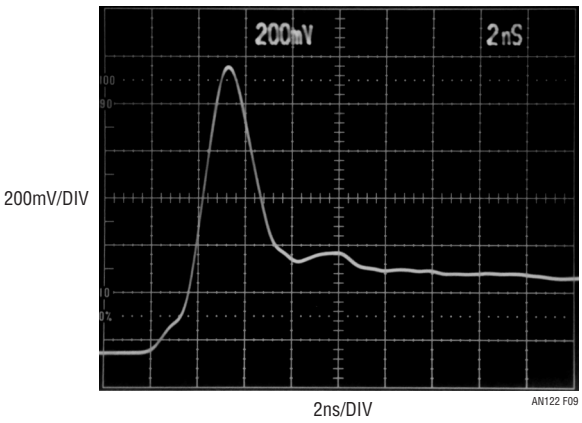


Figure 9. "Diode Number 2" peaks ≈750mV before settling in 6ns... > 2x steady state forward voltage.

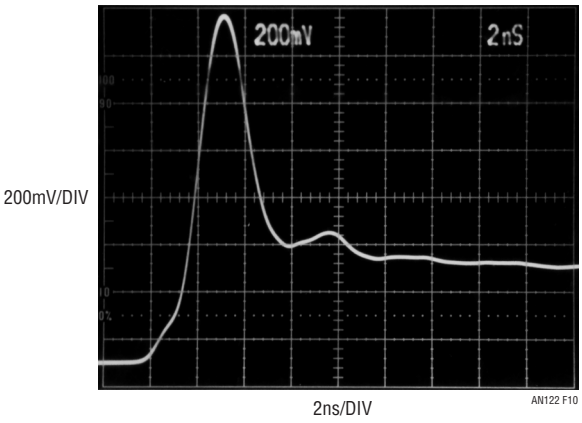


Figure 10. "Diode Number 3" peaks 1V above nominal 400mV VFWD, a 2.5x error.

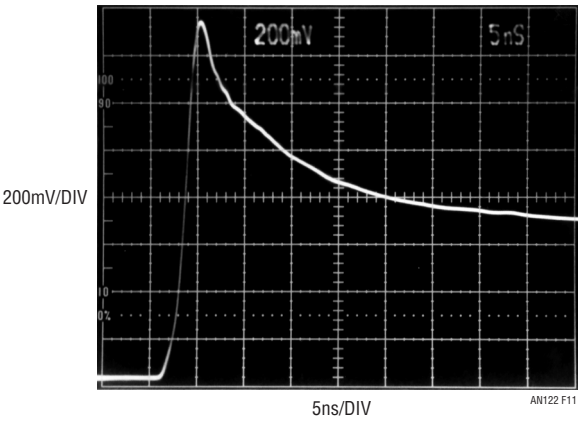


Figure 11. "Diode Number 4" peaks ≈750mV with lengthy (note horizontal 2.5x scale change) tailing towards VFWD value.

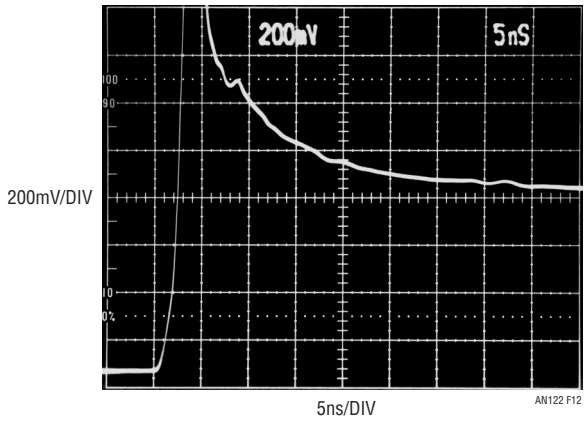


Figure 12. "Diode Number 5" peaks offscale with extended tailing (note horizontal slower scale compared to Figures 8 thru 10).

is deceptively simple in appearance. In particular, the current step must have an exceptionally fast, high-fidelity transition and faithful turn-on time determination requires substantial measurement bandwidth.

Detailed Measurement Scheme

A more detailed measurement scheme appears in Figure 4. Necessary performance parameters for various elements are called out. A subnanosecond rise time pulse generator, 1A, 2ns rise time amplifier and a 1GHz oscilloscope are required. These specifications represent realistic operating conditions; other currents and rise times can be selected by altering appropriate parameters.

The pulse amplifier necessitates careful attention to circuit configuration and layout. Figure 5 shows the amplifier includes a paralleled, Darlington driven RF transistor output stage. The collector voltage adjustment ("rise time trim") peaks Q4 to Q6 FT; an input RC network optimizes output pulse purity by slightly retarding input pulse rise time to within amplifier passband. Paralleling allows Q4 to Q6 to operate at favorable individual currents, maintaining bandwidth. When the (mildly interactive) edge purity and rise time trims are optimized, Figure 6 indicates the amplifier produces a transcendently clean 2ns rise time output pulse devoid of ringing, alien components or post-transition excursions. Such performance makes diode turn-on time testing practical.[1]

Figure 7 depicts the complete diode forward turn-on time measurement arrangement. The pulse amplifier, driven by a sub-nanosecond pulse generator, drives the diode under test. A Z0 probe monitors the measurement point and feeds a 1GHz oscilloscope.[2, 3, 4]

Diode Testing and Interpreting Results

The measurement test fixture, properly equipped and constructed, permits diode turn-on time testing with excellent time and amplitude resolution.[5] Figures 8 through 12 show results for five different diodes from various manufacturers. Figure 8 (Diode Number 1) overshoots steady state forward voltage for 3.6ns, peaking 200mV. This is the best performance of the five. Figures 9 through 12 show increasing turn-on amplitude and time which are detailed in the figure captions. In the worst cases, turn-on amplitudes exceed nominal clamp voltage by more than 1V while turn-on times extend for tens of nanoseconds. Figure 12 culminates this unfortunate parade with huge time and amplitude errors. Such errant excursions can and will cause IC regulator breakdown and failure. The lesson here is clear. Diode turn-on time must be characterized and measured in any given application to insure reliability.

Notes

[1] An alternate pulse generation approach appears in Linear Technology *Application Note 122*, Appendix F, "Another Way to Do It."

[2] Z0 probes are described in Linear Technology *Application Note 122* Appendix C, "About Z0 Probes." See also References 27 thru 34.

[3] The subnanosecond pulse generator requirement is not trivial. See Linear Technology *Application Note 122* Appendix B, "Subnanosecond Rise Time Pulse Generators For The Rich and Poor."

[4] See Linear Linear Technology *Application Note 122* Appendix E, "Connections, Cables, Adapters, Attenuators, Probes and Picoseconds" for relevant commentary.

[5] See Linear Technology *Application Note 122* Appendix A, "How Much Bandwidth is Enough?" for discussion on determining necessary measurement bandwidth.

LTM8032, continued from page 33

amount of ambient noise in the room. Figure 3 shows the noise spectrum in the chamber without any devices running. This can be used to determine the actual noise produced by the DUT.

Figure 4 shows the worst case LTM8032 emissions plot, which occurs at maximum power out, 10V at 2A, from the maximum input voltage, 36V. There are two traces in the plot, one for the vertical and horizontal orientations of the test lab's receiver antenna. As shown in the figure, the LTM8032 easily meets the CISPR 22 class B limits, with 20db of margin for most of the frequency spectrum, with either antenna orientation.

Conclusion

The LTM8032 switching step-down regulator is both easy to use and quiet, meeting the radiated emissions requirements of CISPR22 and EN55022 class B by a wide margin.

Authors can be contacted at (408) 432-1900

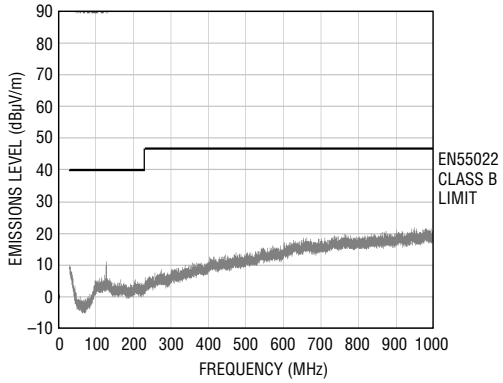


Figure 3. The baseline measurement of ambient noise in the 5-meter chamber (no devices operating)

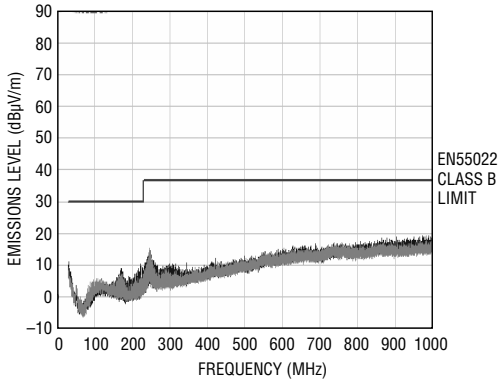


Figure 4. The LTM8032 emissions for 20W out, 36V_{IN}

775 Nanovolt Noise Measurement for a Low Noise Voltage Reference

Quantifying Silence

by Jim Williams

Introduction

Frequently, voltage reference stability and noise define measurement limits in instrumentation systems. In particular, reference noise often sets stable resolution limits.

Reference voltages have decreased with the continuing drop in system power supply voltages, making reference noise increasingly important. The compressed signal processing range mandates a commensurate reduction in reference noise to maintain resolution. Noise ultimately translates into quantization uncertainty in ADCs, introducing jitter in applications such as scales, inertial navigation systems, infrared thermography, DVMs and medical imaging apparatus.

A new low voltage reference, the LTC6655, has only 0.3ppm (775nV) noise at $2.5V_{OUT}$. Table 1 lists salient specifications in tabular form. Accuracy and temperature coefficient are characteristic of high grade, low voltage references. 0.1Hz to 10Hz noise, particularly noteworthy, is unequalled by any low voltage electronic reference.

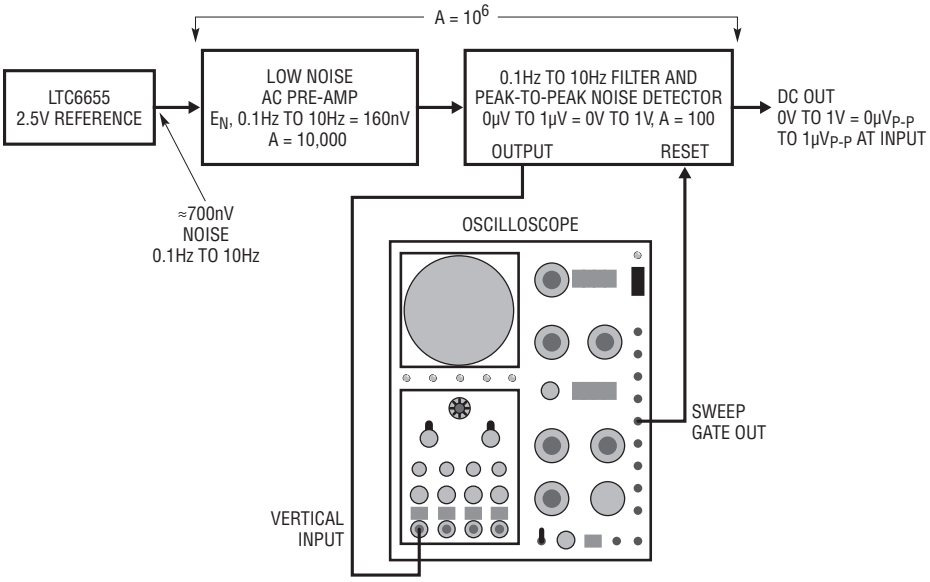


Figure 1. Conceptual 0.1Hz to 10Hz noise testing scheme includes low noise preamplifier, filter and peak-to-peak noise detector. Pre-amplifier's 160nV noise floor, enabling accurate measurement, requires special design and layout techniques.

Noise Measurement

Special techniques are required to verify the LTC6655's extremely low noise. Figure 1's approach appears innocently straightforward but practical implementation represents a high order difficulty measurement. This 0.1Hz to 10Hz noise testing scheme includes a low noise preamplifier, filters and a peak-to-peak noise detector. The preamplifiers 160nV noise floor, enabling accurate measurement, requires special design and layout techniques. A forward gain of 10^6 permits readout by conventional instruments.

Figure 2's detailed schematic reveals some considerations required to achieve the 160nV noise floor. The references' DC potential is stripped by the 1300µF, 1.2k resistor combination; AC content is fed to Q1. Q1-Q2, extraordinarily low noise JFETs, are DC stabilized by A1, with A2 providing a single-ended output. Resistive feedback from A2 stabilizes the configuration at a gain of 10,000. A2's

Table 1. LTC6655 reference tabular specifications. The LTC6655 accuracy and temperature coefficient are characteristic of high grade, low voltage references. 0.1Hz to 10Hz noise, particularly noteworthy, is unequalled by any low voltage electronic reference.

SPECIFICATION	LIMITS
Output Voltages	1.250, 2.048, 2.500, 3.000, 3.300, 4.096, 5.000
Initial Accuracy	0.025%, 0.05%
Temperature Coefficient	2ppm/°C, 5ppm/°C
0.1Hz to 10Hz Noise	0.775µV at V_{OUT} = 2.500V, Peak-to-Peak Noise is within this Figure in 90% of 1000 10-Second Measurement Intervals
Additional Characteristics	5ppm/V Line Regulation, 500mV Dropout, Shutdown Pin, I_{SUPPLY} = 5mA, $V_{IN} = V_O + 0.5V$ to $13.2V_{MAX}$, $I_{OUT(SINK/SOURCE)}$ = ±5mA, $I_{SHORT-CIRCUIT}$ = 15mA.

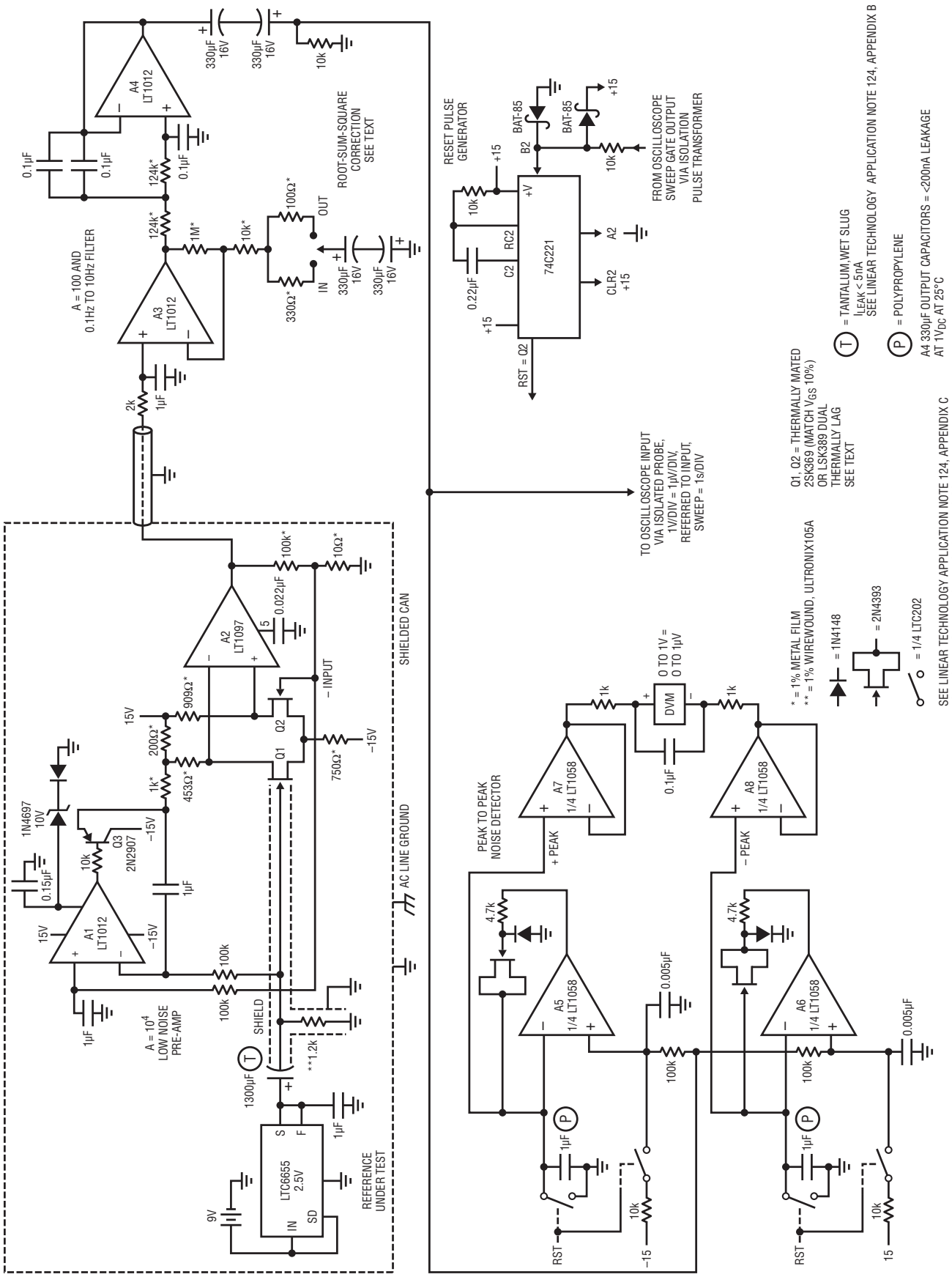


Figure 2. Detailed noise test circuitry. Thermally lagged Q1-Q2 low noise JFET pair is DC stabilized by A1-Q3; A2 delivers A = 10,000 preamplifier output. A3-A4 form 0.1Hz to 10Hz, A = 100, bandpass filter; total gain referred to pre-amplifier input is 10^6. Peak-to-peak noise detector, reset by monitoring oscilloscope sweep gate, supplies DVM output.

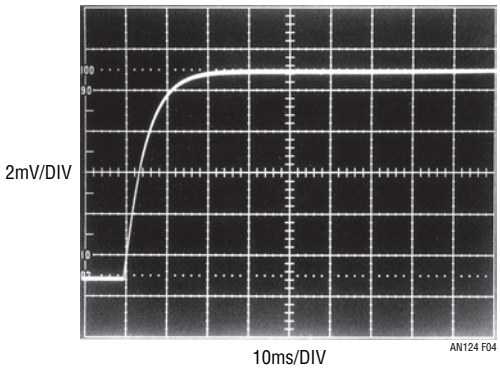


Figure 3. Preamplifier rise time measures 10ms; indicated 35Hz bandwidth ensures entire 0.1Hz to 10Hz noise spectrum is supplied to succeeding filter stage.

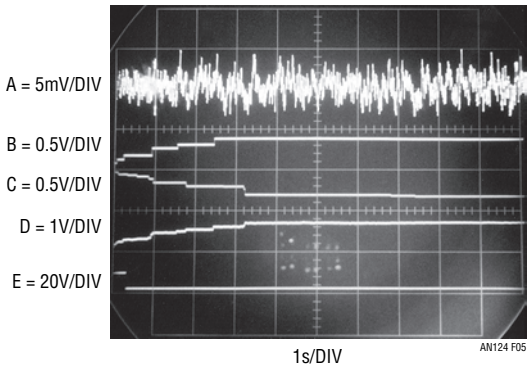


Figure 4. Waveforms for peak-to-peak noise detector include A3 input noise signal (trace A), A7 (trace B) positive/A8 (trace C) negative peak detector outputs and DVM differential input (trace D). Trace E's oscilloscope supplied reset pulse lengthened for photographic clarity.

output is routed to amplifier-filter A3-A4 which provides 0.1Hz to 10Hz response at a gain of 100. A5-A8 comprise a peak-to-peak noise detector read out by a DVM at a scale factor of 1 volt/microvolt. The peak-to-peak noise detector provides high accuracy measurement, eliminating tedious interpretation of an oscilloscope display. Instantaneous noise value is supplied by the indicated output to a monitoring oscilloscope. The 74C221 one-shot, triggered by the oscilloscope sweep gate, resets the peak-to-peak noise detector at the end of each oscilloscope 10-second sweep.

Numerous details contribute to the circuit's performance. The 1300µF capacitor, a highly specialized type, is selected for leakage in accordance with the procedure given in Appendix B. Furthermore, it, and its associated low noise 1.2k resistor, are fully shielded against pick-up. FETs Q1 and Q2 differentially feed A2, forming a simple low noise op amp. Feedback, provided by the 100k-10Ω pair, sets closed loop gain at 10,000. Although Q1 and Q2 have extraordinarily low noise characteristics, their offset and drift are uncontrolled. A1 corrects these deficiencies by adjusting Q1's channel current via Q3 to minimize the Q1-Q2 input difference. Q1's skewed drain values ensure that A1 is able to capture the offset. A1 and Q3 supply whatever current is required into Q1's channel to force offset within about 30µV. The FETs' V_{GS} can vary over a 4:1 range. Because of this, they must be selected for 10% V_{GS} matching. This matching allows A1 to capture the offset without introducing significant noise. Q1 and Q2 are thermally mated and lagged in epoxy at a time constant much greater than A1's DC stabilizing loop roll-off, preventing offset instability and hunting. The entire A1-Q1-Q2-A2 assembly and the reference under test are completely enclosed within a shielded can.[1] The reference is powered by a 9V battery to minimize noise and insure freedom from ground loops.

Peak-to-peak detector design considerations include JFETs used as peak trapping diodes to obtain lower leakage than afforded by conventional diodes. Diodes at the FET gates clamp reverse voltage, further minimizing leakage.[2] The peak storage capacitors highly asymmetric charge-discharge profile necessitates the low dielectric absorption polypropelene capacitors specified.[3] Oscilloscope connections via galvanically isolated links prevent

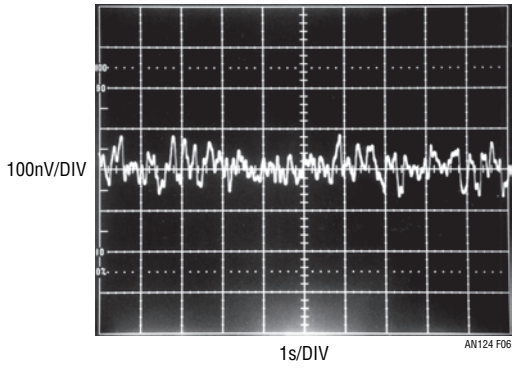


Figure 5. Low noise circuit/layout techniques yield 160nV 0.1Hz to 10Hz noise floor, ensuring accurate measurement. Photograph taken at Figure 3's oscilloscope output with 3V battery replacing LTC6655 reference. noise floor adds ≈2% error to expected LTC6655 noise figure due to root-sum-square noise addition characteristic; correction is implemented at Figure 2's A3.

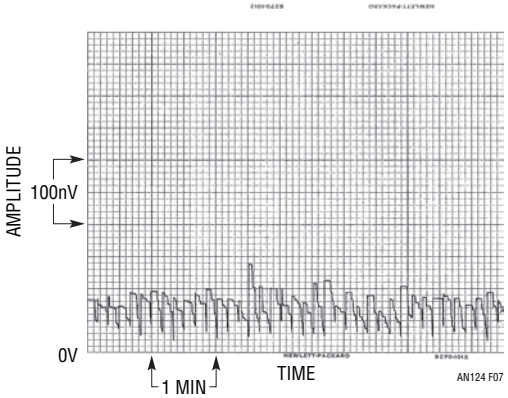


Figure 6. Peak-to-peak noise detector output observed over six minutes shows <160nv test circuit noise. Resets occur every 10 seconds. 3V battery biases input capacitor, replacing LTC6655 for this test.

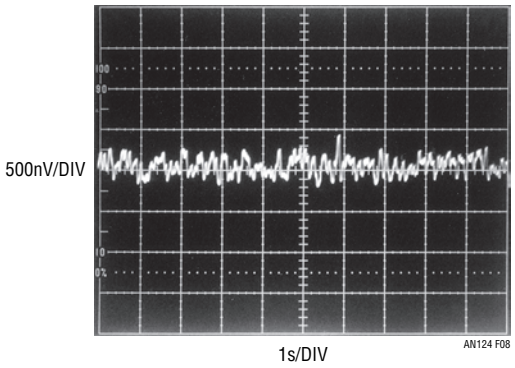


Figure 7. LTC6655 0.1Hz to 10Hz noise measures 775nV in 10-second sample time.

ground loop induced corruption. The oscilloscope input signal is supplied by an isolated probe; the sweep gate output is interfaced with an isolation pulse transformer. For more details, see Linear Technology Application Note 124, Appendix C.

Noise Measurement Circuit Performance

Circuit performance must be characterized prior to measuring LTC6655 noise. The preamplifier stage is verified for >10Hz bandwidth by applying a 1µV step at its input (reference disconnected) and monitoring A2's output. Figure 3's 10ms rise time indicates 35Hz response, insuring the entire 0.1Hz to 10Hz noise spectrum is supplied to the succeeding filter stage.

Figure 4 describes peak-to-peak noise detector operation. Waveforms include A3's input noise signal (Trace A), A7 (Trace B) positive/A8 (Trace C) negative peak detector outputs and DVM differential input (Trace D). Trace E's oscilloscope supplied reset pulse has been lengthened for photographic clarity.

Circuit noise floor is measured by replacing the LTC6655 with a 3V battery stack. Dielectric absorption effects in the large input capacitor require a 24-hour settling period before measurement. Figure 5, taken at the circuit's oscilloscope output, shows 160nV 0.1Hz to 10Hz noise in a 10 second sample window. Because noise adds in root-sum-square fashion, this represents about a 2% error in the LTC6655's expected 775nV noise figure. This term is accounted for by placing Figure 2's "root-sum-square correction" switch in the appropriate position during reference testing. The resultant 2% gain attenuation first order corrects LTC6655 output noise reading for the circuit's 160nV noise floor contribution. Figure 6, a strip-chart recording of the peak-to-peak noise detector output over six minutes, shows less than 160nV test circuit noise.[4] Resets occur every 10 seconds. A 3V battery biases the input capacitor, replacing the LTC6655 for this test.

Figure 7 is LTC6655 noise after the indicated 24-hour dielectric absorption soak time. Noise is within 775nV peak-to-peak in this 10 second sample window with the root-sum-square correction enabled. The verified, extremely low circuit noise floor makes it highly likely this data is valid. In closing, it is worth mention that the approach taken is applicable to measuring any 0.1Hz to 10Hz noise source, although the root-sum-square error correction coefficient should be re-established for any given noise level.

Notes

[1] The preamplifier structure must be carefully prepared. See Appendix A in Linear Technology Application Note 124, "Mechanical and Layout Considerations," for detail on preamplifier construction.

[2] Diode-connected JFETs' superior leakage derives from their extremely small area gate-channel junction. In general, JFETs leak a few picoamperes (25°C) while common signal diodes (e.g. 1N4148) are about 1,000× worse (units of nanoamperes at 25°C).

[3] Teflon and polystyrene dielectrics are even better but the Real World intrudes. Teflon is expensive and excessively large at 1µF. Analog types mourn the imminent passing of the polystyrene era as the sole manufacturer of polystyrene film has ceased production.

[4] That's right, a *strip-chart recording.* Stubborn, locally based aberrants persist in their use of such archaic devices, forsaking more modern alternatives. Technical advantage could account for this choice, although deeply seated cultural bias may be indicated.

LT3971/91, continued from page 5

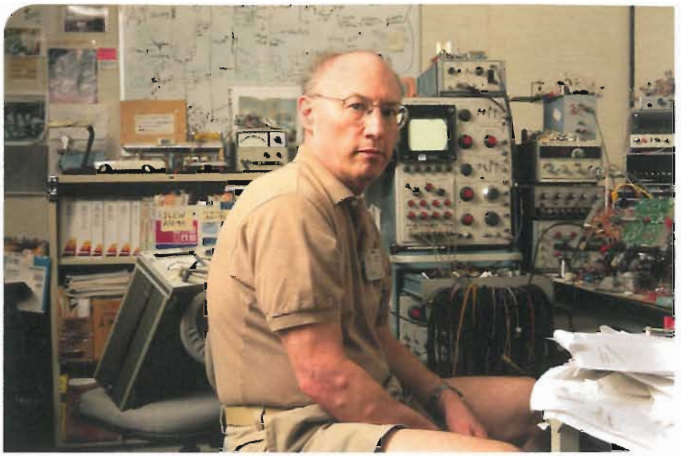
and external clock synchronization features, and comes in a 10-pin MSOP or 3mm × 3mm DFN package, both with an exposed ground pad.

The LT3991 has a typical minimum switch on time of 110ns at room and 150ns at 85°C, which allow higher switching frequencies for large step-down ratios when compared to other parts with similar high input voltage ratings. Figure 8 shows a 48V input to a 3.3V output application with a switching frequency of 300kHz. The 10µH inductor and 47µF output capacitor yield a small overall solution size. The output capacitor can be a small ceramic capacitor, as opposed to a tantalum capacitor, because the LT3991 does not need any output capacitor ESR for stability.

Conclusion

The LT3971 and LT3991 are ultralow quiescent current regulators that can regulate a 12V input to a 3.3V output during no load conditions with only 2.8µA of input current. Light load operation with single current pulses keeps the output voltage ripple to less than 15mV. These buck regulators can also provide up to 1.2A of output current. The LT3971 and LT3991 are well suited for keep-alive and remote monitoring systems with low duty cycle, high current, pulsed outputs. The wide input range from 4.3V up to 38V for the LT3971, and 55V for the LT3991, along with the programmable input voltage enable threshold feature, allow these converters to be driven from a wide range of input sources. The ultralow quiescent current performance of the LT3971 and LT3991 make them great choices for battery-operated systems where power conservation is critical.

In this issue...



In the lab.

JIM WILLIAMS REMEMBERED

I have known Jim Williams for 30 years. I have known him as the consummate engineer, scientist, writer, humorist, and family man. In all areas that Jim ventured, he excelled. His combination of personal integrity, drive and humble interaction with other people drew many friends, both for his writing and personal interactions.

Jim's intuitive understanding of electronics enabled him to design complicated circuits in his head, which he tested with real parts to prove the circuits. The ability to design circuits also requires analysis of the results of the testing. His strong analytical ability ensured test results were correct and circuits were well understood.

Jim took his developments and turned them into words for publication. He helped engineers of all ages understand circuits intuitively like he did. There are few sources for advanced circuit understanding and design—especially the way it was taught by Jim. His circuits and his writings provided insight so that other people could approach his understanding of design. In all the time I've known Jim, I have never known him to refuse to help someone with a circuit.

While Jim's vocation, avocation and hobby were electronics, he had a great sense of humor and art. His electronic sculptures are unique, beautiful and functional. He built these structures (with much cursing) and careful selection of aesthetically pleasing functional parts. Beyond his art, he had a great sense of humor, which was often foisted on his friends, myself included.

In his personal life, he was a dedicated father to his son Michael and husband to his wife Siu. Both of these people were very much a part of his life.

A successful poet is the rarest of all vocations. Jim Williams was unique: a poet who wrote in electronics.

—Bob Dobkin